Is Application dependent forecasting of microprocessors possible?

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Abstract

The application of microprocessor is expanding vastly through majority of products. Technological advancements in the microprocessor industry are benchmarked mainly against their performance. This paper is an analysis of possibility for grouping and forecasting microprocessors based on their application. This would create the opportunity for better forecasting of their performance or characteristics.

Hypothesis

Application dependent forecasting of microprocessors are not possible based on the historical product specification information.

Analysis

Following previous forecasting studies using TFDEA[1][2], I like to first forecast microprocessor performance in general and then, if possible, based on the market they serve. It would be useful if we could segment the collected microprocessors and try to forecast the trajectory specific to each group of microprocessors. Hence, this paper tries to explore the possibility of conducting forecasting for each group of microprocessors (Server/ Desktop).

As industry[3][4] claims, server and desktop processors are not differentiated based on performance. The most important differentiating factors are including superior reliability, dependability, self-

correction and capability to handle higher trafficking[5][6]. My goal of this statistical analysis is to accept or reject this hypothesis.

In an earlier study, my team and I collected and analyzed a group of 192 processors released over the past 15 years by various manufacturers. Using TFDEA (Technology Forecasting using Data Envelopment Analysis) as our forecasting methodology, we were able to find a Rate of Change of approximately 24.4% (Appendix I – Dataset and TFDEA forecasting result). This rate of change indicates that the future competitive processors either improve their input variables by 24.4% for the similar performance or improve their output performance variable by 24.4% for the similar input per year (Constant Return to Scale was used).

As an alternative forecasting method, I conduct multiple regression analysis to find the best regression hyper plane predicting the performance of the future processors in general. Then, using Discriminant Analysis, explore the possibility of creating forecasting hyper-plane for each group of processors (e.g. Server vs. Desktop market). The input and output variables used in this study are listed in Table 2 - Input & Output variables in Appendix I – Dataset and TFDEA forecasting result.

Regression Analysis

Stepwise I) Regression Hyperplane using Stepwise model with BIC Criterion:

$$Y_{Y\_fp\_Gust} = -7.42 + 34.14\,X_{Core} + 5.52\,X_{X\_Rec\_FS} + 11.27\,X_{X\_TransPC} + 0.15\,X_{X\_DieSize} - 23.86\,X_{X\_Transistor}$$

Equation 1

Based on the linear model analysis result, this regression formula describes 80% of the performance variance (Based on Multiple R-squared: 0.8101 and Adjusted R-squared: 0.805), and it's statistically significant (p-value: < 2.2e-16) (Appendix IV - Linear Model for the result of BIC stepwise regression).

Stepwise II) Regression Hyper-plane using Stepwise model with AIC Criterion:

$$Y_{Y\_fp\_Gust} = 116.27 + 36.39\,X_{Core} + 5.48\,X_{X\_Rec\_FS} + 11.92\,X_{X\_TransPC} + 0.21\,X_{X\_DieSize} - 43.44\,X_{X\_Transistor} + 0.014\,X_{Clock} - 0.14\,X_{X\_Power}$$

Equation 2

And the linear model analysis of this regression formula suggests that it again describes 80% of the output performance variability (Multiple R-red: 0.8164, Adjusted R-squared: 0.8094). While this formula is statistically significant (p-value: < 2.2e-16)(Appendix VI - Linear Model for the result of AIC stepwise regression), the addition of Clock and power parameter has provided little value. Hence, I select the Equation 1 as the preferred performance forecasting formula.

Result Comparison

Based on the TFDEA analysis, the performance of microprocessors will be enhanced by 24.45% per year(Appendix I – Dataset and TFDEA forecasting result) (as the forecasting is Constant Return to Scale the Rate of Change can be applied to both input or output). On the other hand, According to the Regression forecasting in Equation 1 for the inputs variables that are 24.4% enhanced (leveling it with TFDEA, so we can compare them), the output performance ($Y_{Y\_fp\_Gust}$) is approximately 20% better. Table 1 depicts a sample performance output ($Y_{Y\_fp\_Gust}$) for the two forecasting method based on Intel Core i7-3770T (a competitive cpu released in 2012 with the output performance of 220.89). Based on these results, there is a 3.69% difference between our TFDEA and Regression forecasted performance output.

Intel Core i7-3770T	Rate of Change	2013 Performance Forecast
TFDEA	1.244552	274.9090913
Regression	1.200236	265.120212
Difference		3.69%

Table 1 – Performance calculation comparison (Intel Core i7-3770T)

Market Segmentation Evaluation (1998 to 2012)

To evaluate my hypothesis, I like to conduct Discriminant Analysis on the collected information on the microprocessors released from 1998. To perform this analysis, the data should confirm segmentation. I.e. the microprocessors should clearly separate at least based on one of their characteristics in our dataset. For this study, I researched every processor in the dataset and added a new field, Type, to categorize their use based on the original purpose of their design (1: designed for server vs. 2: designed for desktop). For evaluation of whether these processors are any different in their characteristics, here I plot a matrix of the processors specifications based on their Type:

```
> install.packages("lattice")
> require(lattice)
> splom(cpuTPS[1:11], groups = cpuTPS$Type)
```

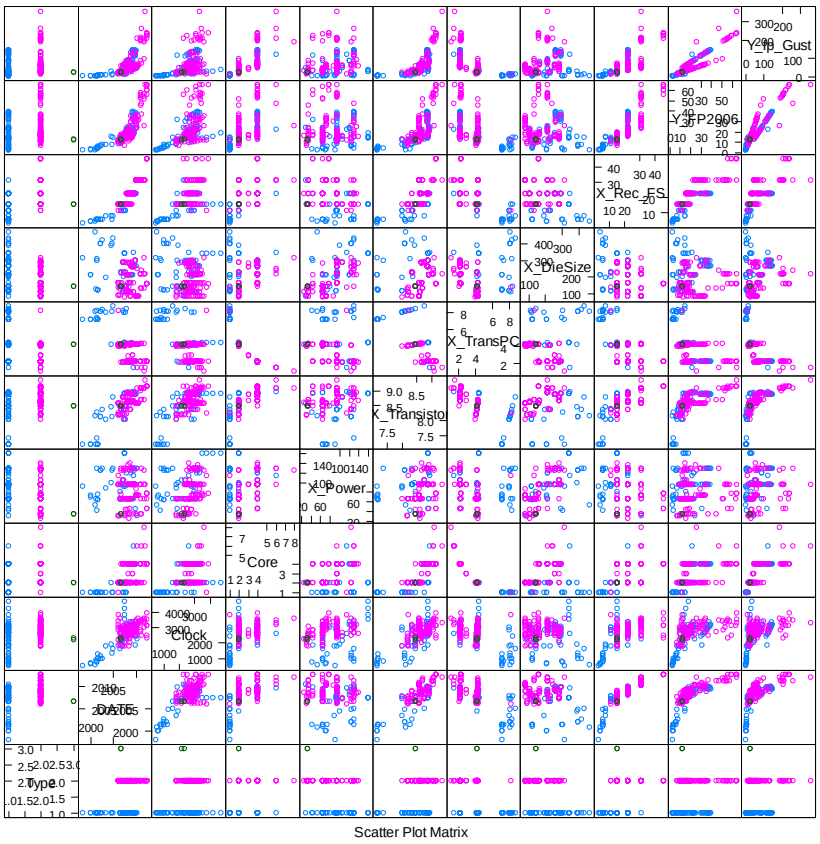


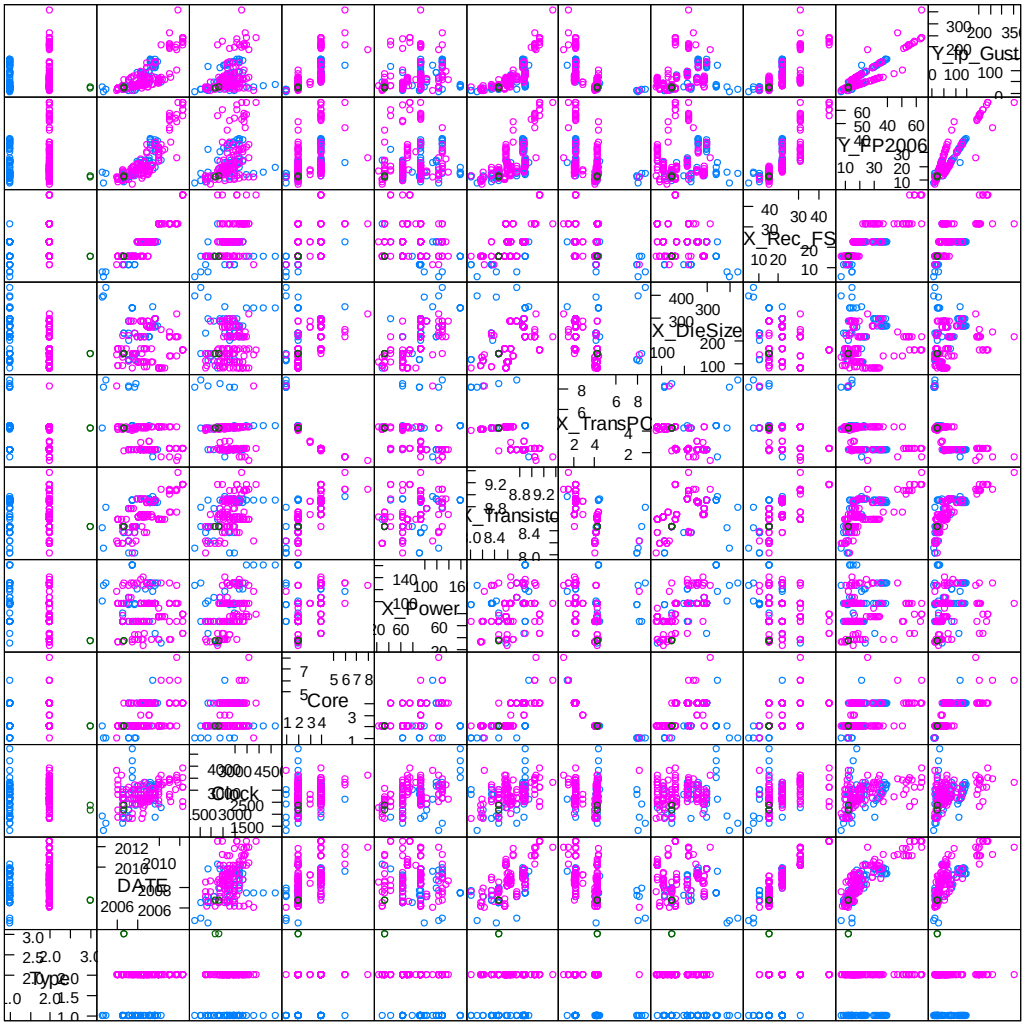
Figure 1 - Scatter Plot of processors' characteristics (1998 to 2012)

As observed in Figure 1 plot matrix, data is quite polluted. Other than the plot based on Type variable (which we segmented and not part of the analysis), none of the plots are indicating a clear grouping. Reviewing the collected data, as there are no desktop processor in the dataset, to perform an analysis for a priod that both type of processors existed, I am going to perform the analysis on the processors from 2005 to 2012. This could help us depart from a data that doesn't reflect a more recent trend.

Market Segmentation Evaluation (2005 to 2012)

As prior to this time there was no clear separation of the processors application (server vs. desktop) I want to see if there is a trend change from 2005 were there are more variety of processors in the market. My goal is to see if I can find any grouping of the data that can possibly allow Discriminant Analysis and reject the hypothesis.

```
> cpu04 <- read.csv("c:/R/cpu04.csv")
> splom(cpu04[1:11], groups = cpu04$Type)
```



Scatter Plot Matrix

Figure 2 - Scatter Plot of processors' characteristics (2005-2012)

As observed in Figure 2, even this subset of data doesn't show any grouping of the processors based on their application (server vs. desktop use).

Market Segmentation Evaluation (2008 to 2012)

This time I'm removing all the processors manufactured prior to 2008. CPU manufacturing Technology continues to bloom in this era and I simply want to see if there is a separation between the two markets in the more recent processors. Again this is an attempt to discover a grouping between these two groups of processors in the dataset to reject the hypothesis.

```
> splom(cpu08[1:11], groups = cpu08$Type)
```

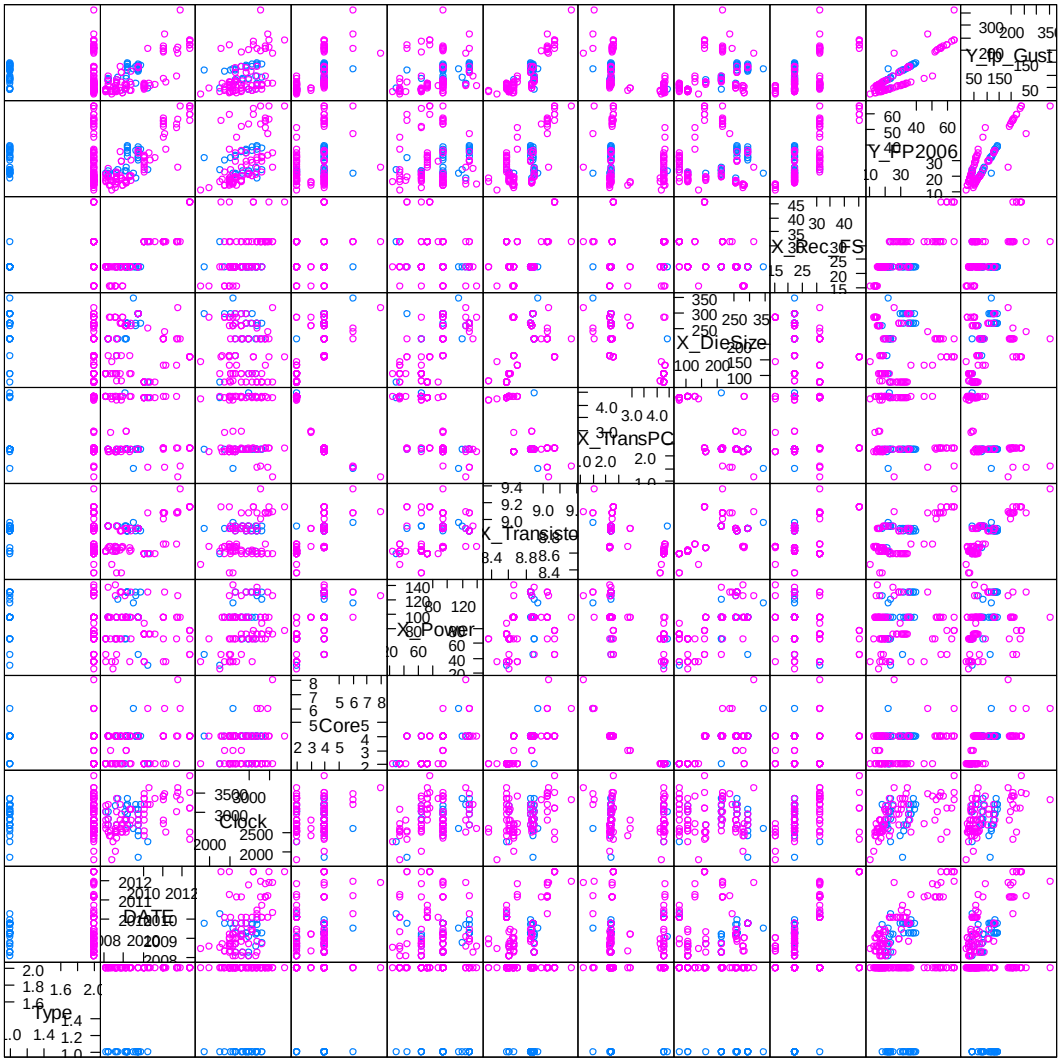


Figure 3 - Scatter Plot of processors' characteristics (2008-2012)

Similar to the other two groups, the plot matrix here doesn't indicate any grouping and depicts that the discriminant analysis cannot be conducted on this dataset as there are no separation of characteristics(that our dataset contains) in these two groups.

Conclusion

In summary, this paper concludes that there is no characteristic considered in dataset that separates the processors in the applications of server and desktop. Neither independent nor dependent variables in this study show any segmentation between the two groups. Since the sample size of the processors in the dataset is close to the population size, therefore we can safely reject the null hypothesis and accept our hypothesis that application dependent forecasting of microprocessors is not possible.

The overall TFDEA forecasting in an earlier study or regression hyper plane found in the stepwise analysis of this paper is the appropriate one for forecasting the performance of both kinds of server and non-server processors.

Bibliography

[1] T. Anderson, R. Färe, S. Grosskopf, L. Inman, and X. Song, "Further examination of Moore's law with data envelopment analysis," *Technological Forecasting and Social Change*, vol. 69, no. 5, pp. 465–477, Jun. 2002.

[2] D.-J. Lim and T. R. Anderson, "An introduction to Technology Forecasting with a TFDEA Excel add-in," in *Technology Management for Emerging Technologies (PICMET), 2012 Proceedings of PICMET '12:*, 2012, pp. 1293 –1298.

[3] MU_Engineer, "Desktop vs Server CPU." TomsHardware, 05-Feb-2011.

[4] "The Difference Between a Server and Desktop CPU | UNIXy." [Online]. Available: http://blog.unixy.net/2009/12/the-difference-between-a-server-and-desktop-cpu/. [Accessed: 18-Mar-2013].

[5] "Difference between Server and Desktop CPU - Web Hosting Talk." [Online]. Available: http://www.webhostingtalk.com/showthread.php?t=868765. [Accessed: 20-Mar-2013].

[6] "ubuntu - difference between server and desktop - Server Fault." [Online]. Available: http://serverfault.com/questions/442962/difference-between-server-and-desktop. [Accessed: 20-Mar-2013].

Appendix I – Dataset and TFDEA forecasting result

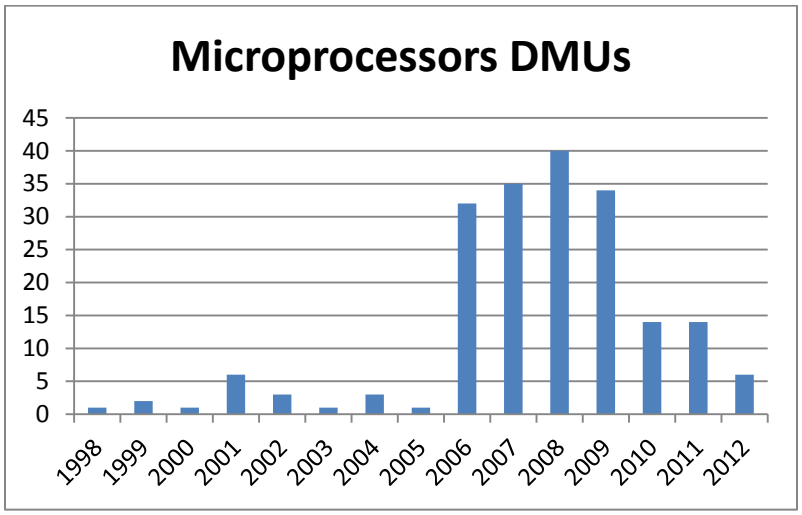


Figure 4 - Concentration of the Microprocessors in the dataset

Inputs								Output
DATE	Clock	Core	power (Watts)	Transistor (Log 10)	Transistor per core (Log 10)	Die Size [mm2]	Reciprocal of Feature Size [µm-1]	Y_fp_Gust

Table 2 - Input & Output variables

$$Y\_fp\_Gust = SPECfp \cdot [p - \alpha \cdot (p - 1)].$$

Equation 3 - MultiCore performance calculation (α=0.1)

Frontier Year	Learning Period	Validation Period	RoC	MAD [years]
2008	1998 – 2008	2008 – 2012	1.466085	0.554220
2009	1998 – 2009	2009 – 2012	1.322422	0.463059
2010	1998 – 2010	2010 – 2012	1.229894	0.864379
2011	1998 – 2011	2011 – 2012	1.219282	1.478995
2012	1998- 2012	2012	1.244552	0.700999

Table 3 - Forecasting result from TFDEA

Rate of Change	1.244552
Standard Deviation	0.093375342
95% Confidence Interval	± 0.02490482

Table 4 - RoC and SD of frontier year 2012

Appendix II - Linear Model Regression Analysis for performance output(Y_fp_Gust)

```
> LinearModel.2 <- lm(Y_fp_Gust ~ Clock + Core + DATE + Type + X_DieSize +
X_Power + X_Rec_FS + X_Transistor + X_TransPC, data=Dataset)

> summary(LinearModel.2)

Call:
lm(formula = Y_fp_Gust ~ Clock + Core + DATE + Type + X_DieSize +
    X_Power + X_Rec_FS + X_Transistor + X_TransPC, data = Dataset)

Residuals:
     Min       1Q   Median       3Q      Max
-108.405  -16.211   -0.135   14.568  158.251

Coefficients:
               Estimate Std. Error t value Pr(>|t|)
(Intercept)   1.282e+03  4.860e+03   0.264 0.792186
Clock         1.336e-02  6.077e-03   2.199 0.029191 *
Core          3.673e+01  4.370e+00   8.405 1.44e-14 ***
DATE         -5.889e-01  2.446e+00  -0.241 0.810019
Type         -7.131e+00  4.580e+00  -1.557 0.121285
X_DieSize     2.042e-01  5.034e-02   4.056 7.51e-05 ***
X_Power      -2.001e-01  1.217e-01  -1.644 0.101896
X_Rec_FS      5.373e+00  5.573e-01   9.642  < 2e-16 ***
X_Transistor -3.840e+01  1.421e+01  -2.703 0.007558 **
X_TransPC     1.060e+01  3.011e+00   3.519 0.000552 ***
---
Signif. codes:  0 '***' 0.001 '**' 0.01 '*' 0.05 '.' 0.1 ' ' 1

Residual standard error: 26.81 on 175 degrees of freedom
  (7 observations deleted due to missingness)
Multiple R-squared: 0.8259, Adjusted R-squared: 0.817
F-statistic: 92.26 on 9 and 175 DF,  p-value: < 2.2e-16

> LinearModel.3 <- lm(Y_FP2006 ~ Clock + Core + DATE + Type + X_DieSize +
X_Power + X_Rec_FS + X_Transistor + X_TransPC, data=cpuws)

> summary(LinearModel.3)
```

Appendix III - Stepwise Analysis using BIC

```
> stepwise(LinearModel.4, direction='forward/backward', criterion='BIC')

Direction:  forward/backward
Criterion:  BIC

Start:  AIC=1586.98
Y_fp_Gust ~ 1

               Df Sum of Sq    RSS    AIC
```

```
+ Core          1    434996 287332 1414.1
+ X_Rec_FS      1    403745 318583 1434.0
+ DATE          1    347013 375315 1465.4
+ X_Transistor  1    337441 384887 1470.3
+ X_TransPC     1    304893 417435 1485.8
+ Clock         1    150517 571811 1546.3
+ X_Power       1     32273 690055 1582.3
+ X_DieSize     1     21722 700606 1585.3
<none>                      722328 1585.9
+ Type          1     15695 706633 1586.9

Step:  AIC=1434.45
Y_fp_Gust ~ Core

               Df Sum of Sq    RSS    AIC
+ X_Rec_FS      1    113713 173620 1322.6
+ DATE          1     54480 232852 1379.0
+ X_Transistor  1     21277 266055 1404.6
+ Clock         1     14576 272756 1409.4
+ X_Power       1      6841 280492 1414.7
+ X_DieSize     1      5859 281473 1415.4
+ X_TransPC     1      4148 283185 1416.6
+ Type          1       690 286642 1418.9
<none>                     319401 1434.5
- Core          1    406989 726390 1587.0

Step:  AIC=1333.01
Y_fp_Gust ~ Core + X_Rec_FS

               Df Sum of Sq    RSS    AIC
+ X_TransPC     1     30655 142965 1290.5
+ X_DieSize     1     20900 152720 1303.2
+ Type          1     11546 162074 1314.6
+ DATE          1      7340 166280 1319.6
+ X_Power       1      4701 168919 1322.6
+ X_Transistor  1      1964 171655 1325.7
+ Clock         1      1894 171726 1325.7
<none>                     183262 1333.0
- Core          1    135929 319191 1434.3
- X_Rec_FS      1    136139 319401 1434.5

Step:  AIC=1299.32
Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC

               Df Sum of Sq    RSS    AIC
+ X_DieSize     1      8535 134430 1284.0
+ Type          1      4116 138849 1290.2
+ X_Power       1      1493 141472 1293.8
+ DATE          1       397 142568 1295.2
+ Clock         1        71 142894 1295.7
+ X_Transistor  1         3 142961 1295.8
<none>                     149643 1299.3
- X_TransPC     1     33619 183262 1333.0
- Core          1    123797 273440 1409.8
- X_Rec_FS      1    165099 314743 1436.8

Step:  AIC=1294.05
```

```
Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize

               Df Sum of Sq    RSS    AIC
+ X_Transistor  1      3561 130869 1284.0
+ Type          1      1869 132561 1286.5
+ DATE          1       670 133760 1288.2
+ X_Power       1        38 134392 1289.1
+ Clock         1        18 134412 1289.2
<none>                     141687 1294.0
- X_DieSize     1      7957 149643 1299.3
- X_TransPC     1     20856 162543 1315.2
- Core          1     53966 195652 1350.8
- X_Rec_FS      1    152640 294327 1429.2

Step:  AIC=1294.12
Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize + X_Transistor


Call:
lm(formula = Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize +
    X_Transistor, data = cpuws)

Coefficients:
 (Intercept)          Core      X_Rec_FS     X_TransPC     X_DieSize
X_Transistor
     -7.4168       34.1436        5.5163       11.2681        0.1509      -
23.8558
```

Appendix IV - Linear Model for the result of BIC stepwise regression

```
> LinearModel.5 <- lm(Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize +
X_Transistor, data=cpuws)

> summary(LinearModel.5)

Call:
lm(formula = Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize +
    X_Transistor, data = cpuws)

Residuals:
    Min      1Q  Median      3Q     Max
-94.241 -14.627  -0.711  14.693 159.598

Coefficients:
              Estimate Std. Error t value Pr(>|t|)
(Intercept)   -7.41678   90.27379  -0.082 0.934609
Core          34.14365    4.23710   8.058  9.1e-14 ***
X_Rec_FS       5.51630    0.45312  12.174  < 2e-16 ***
X_TransPC     11.26811    2.97674   3.785 0.000207 ***
X_DieSize      0.15091    0.03803   3.968 0.000103 ***
X_Transistor -23.85582   10.61560  -2.247 0.025800 *
---
Signif. codes:  0 '***' 0.001 '**' 0.01 '*' 0.05 '.' 0.1 ' ' 1
```

```
Residual standard error: 27.23 on 186 degrees of freedom
Multiple R-squared: 0.8101, Adjusted R-squared: 0.805
F-statistic: 158.7 on 5 and 186 DF,  p-value: < 2.2e-16
```

Appendix V - Stepwise Analysis using AIC

```
> stepwise(LinearModel.4, direction='forward/backward', criterion='AIC')

Direction:  forward/backward
Criterion:  AIC

Start:  AIC=1583.76
Y_fp_Gust ~ 1

               Df Sum of Sq    RSS    AIC
+ Core          1    434996 287332 1407.7
+ X_Rec_FS      1    403745 318583 1427.5
+ DATE          1    347013 375315 1459.0
+ X_Transistor  1    337441 384887 1463.8
+ X_TransPC     1    304893 417435 1479.4
+ Clock         1    150517 571811 1539.8
+ X_Power       1     32273 690055 1575.9
+ X_DieSize     1     21722 700606 1578.8
+ Type          1     15695 706633 1580.5
<none>                     722328 1582.7

Step:  AIC=1428.01
Y_fp_Gust ~ Core

               Df Sum of Sq    RSS    AIC
+ X_Rec_FS      1    113713 173620 1313.0
+ DATE          1     54480 232852 1369.3
+ X_Transistor  1     21277 266055 1394.9
+ Clock         1     14576 272756 1399.7
+ X_Power       1      6841 280492 1405.1
+ X_DieSize     1      5859 281473 1405.7
+ X_TransPC     1      4148 283185 1406.9
+ Type          1       690 286642 1409.2
<none>                     319401 1428.0
- Core          1    406989 726390 1583.8

Step:  AIC=1323.35
Y_fp_Gust ~ Core + X_Rec_FS

               Df Sum of Sq    RSS    AIC
+ X_TransPC     1     30655 142965 1277.7
+ X_DieSize     1     20900 152720 1290.3
+ Type          1     11546 162074 1301.8
+ DATE          1      7340 166280 1306.7
+ X_Power       1      4701 168919 1309.7
+ X_Transistor  1      1964 171655 1312.8
+ Clock         1      1894 171726 1312.9
<none>                     183262 1323.3
- Core          1    135929 319191 1427.9
```

```
- X_Rec_FS      1    136139 319401 1428.0

Step:  AIC=1286.43
Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC

               Df Sum of Sq    RSS    AIC
+ X_DieSize     1      8535 134430 1267.8
+ Type          1      4116 138849 1274.1
+ X_Power       1      1493 141472 1277.7
+ DATE          1       397 142568 1279.1
+ Clock         1        71 142894 1279.6
+ X_Transistor  1         3 142961 1279.7
<none>                     149643 1286.4
- X_TransPC     1     33619 183262 1323.3
- Core          1    123797 273440 1400.2
- X_Rec_FS      1    165099 314743 1427.2

Step:  AIC=1277.94
Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize

               Df Sum of Sq    RSS    AIC
+ X_Transistor  1      3561 130869 1264.7
+ Type          1      1869 132561 1267.2
+ DATE          1       670 133760 1268.9
+ X_Power       1        38 134392 1269.8
+ Clock         1        18 134412 1269.8
<none>                     141687 1277.9
- X_DieSize     1      7957 149643 1286.4
- X_TransPC     1     20856 162543 1302.3
- Core          1     53966 195652 1337.9
- X_Rec_FS      1    152640 294327 1416.3

Step:  AIC=1274.8
Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize + X_Transistor

               Df Sum of Sq    RSS    AIC
+ Clock         1      1746 129122 1264.1
+ Type          1      1532 129337 1264.4
+ DATE          1       100 130769 1266.5
+ X_Power       1         3 130866 1266.7
<none>                     137941 1274.8
- X_Transistor  1      3745 141687 1277.9
- X_TransPC     1     10627 148568 1287.0
- X_DieSize     1     11679 149621 1288.4
- Core          1     48158 186099 1330.3
- X_Rec_FS      1    109916 247857 1385.3

Step:  AIC=1271.8
Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize + X_Transistor +
    Clock

               Df Sum of Sq    RSS    AIC
+ X_Power       1      1608 127514 1263.7
+ Type          1      1439 127683 1264.0
+ DATE          1         0 129122 1266.1
<none>                     134392 1271.8
- Clock         1      3550 137941 1274.8
```

```
- X_Transistor  1      6890 141281 1279.4
- X_TransPC     1     11093 145485 1285.0
- X_DieSize     1     14400 148791 1289.3
- Core          1     50081 184473 1330.6
- X_Rec_FS      1    110901 245293 1385.3

Step:  AIC=1272.33
Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize + X_Transistor +
    Clock + X_Power


Call:
lm(formula = Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize +
    X_Transistor + Clock + X_Power, data = cpuws)

Coefficients:
 (Intercept)          Core      X_Rec_FS     X_TransPC     X_DieSize
X_Transistor         Clock       X_Power
   116.27188      36.39210       5.48146      11.92326       0.21004     -
43.44031       0.01405      -0.13968
```

Appendix VI - Linear Model for the result of AIC stepwise regression

```
> LinearModel.7 <- lm(Y_fp_Gust ~ Core + X_Rec_FS +X_TransPC +X_DieSize
+X_Transistor +Clock +X_Power, data=cpuws)

> summary(LinearModel.7)

Call:
lm(formula = Y_fp_Gust ~ Core + X_Rec_FS + X_TransPC + X_DieSize +
    X_Transistor + Clock + X_Power, data = cpuws)

Residuals:
     Min       1Q   Median       3Q      Max
-109.494  -15.105   -1.818   15.437  159.863

Coefficients:
               Estimate Std. Error t value Pr(>|t|)
(Intercept)  116.271876 102.421690   1.135  0.25776
Core          36.392098   4.375933   8.316 1.97e-14 ***
X_Rec_FS       5.481464   0.451091  12.152  < 2e-16 ***
X_TransPC     11.923258   2.964376   4.022 8.41e-05 ***
X_DieSize      0.210041   0.049494   4.244 3.48e-05 ***
X_Transistor -43.440307  13.147322  -3.304  0.00115 **
Clock          0.014047   0.005796   2.423  0.01635 *
X_Power       -0.139681   0.117456  -1.189  0.23589
---
Signif. codes:  0 '***' 0.001 '**' 0.01 '*' 0.05 '.' 0.1 ' ' 1

Residual standard error: 26.92 on 184 degrees of freedom
Multiple R-squared: 0.8164, Adjusted R-squared: 0.8094
F-statistic: 116.9 on 7 and 184 DF,  p-value: < 2.2e-16
```