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Technology forecasting for DRAM

Course Title: Technology Forecasting
Course Number: ETM 532 / 632
Instructor: Dr. Jisun Kim
Term: Winter
Year: 2013

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1 Executive summary

Some analysts fear that the semiconductor technology has entered, or is about to enter, the mature stage of its life cycle. In this paper, the authors' focus is to study a very active sector of the semiconductor industry, the dynamic-random-access memory (DRAM) technology. A fair understanding of the history, applications, limitations and complementary technologies was conducted to suggest a reasonable forecast for the upcoming near future of the technology. The scope was to answer the question of whether, or not, the DRAM technology has reached its maturity and soon needs to be replaced by a newer one. Literature review, experts' opinion, and the suitable computational method TFDEA, were utilized to conclude the following; The DRAM technology can continue its current trend in the short and medium future terms as long as the improvements in the supportive technologies contribute to make these projections a reality. Should the limits of physics become a definite roadblock, other prospective emerging technologies are undergoing advanced research efforts and may be proposed as an alternative to carry on with the better results delivery trend.

2 Introduction

The last few decades of the 20th century have been characterized by a blast of innovations that covered the majority fields of the vast science arena. Some of those inventions were incremental while others were destructive in nature and all of them led to a totally different way of living our lives. We started that century with an embryonic stage of airplanes, automobiles, and wireless signaling. And, at the other hand, we withdrew from it with the mind dazzling spacecraft, personal and industrial computer, and the almost uninterrupted internet access. Those were few samples of the endless list that we truly benefited from, enjoyed for granted, and ridiculously complained about for not being able to deliver more.

The semiconductor technology was not an exception, but indeed it was at the center stage of all the activities and mainly in the last three to four decades. The industry overcame barriers soon as they were encountered, and the progress in all performance dimensions was surprisingly shocking. As Ayres [1] indicates, "It is probably safe to say that any truly constraining limits to semiconductor performance are still quite far away." Some analysts fear that the semiconductor technology has entered, or is about to enter, the mature stage of its life cycle. They back their claim by various noticeable evidences such as the incrementing cost of R&D, the low threat of new entrants due to very challenging entry barriers, and the "increasing movement toward vertical integration" [2].

In this paper, the authors will study a very active contributor sector of the semiconductor industry, the dynamic-random-access memory (DRAM) technology. A fair understanding of the history, applications, limitations and complementary technologies will be conducted to suggest a reasonable forecast for the near future of the technology in order to answer the question of whether, or not, the DRAM technology has reached its maturity and soon needs to be replaced by a newer one. Literature review, experts' opinion, when available, and a suitable computational method, the TFDEA, will be utilized to fulfill the goal of this work.

3 DRAM Background & Literature Review

3.1 The DRAM technology

The initiation and arrival to the market of the DRAM could be dated back to the year of 1970 when the 1-Kbit, three transistors cell, chip was introduced by Intel Corporation. Three years later, the 4-Kbit, 1 transistor cell, chip was introduced to start a new saga. The commodity continued to quadruple, in capacity size, every three years and maintained, at least, a solid 10% share of the total semiconductor industry [3] [4]. The $30-Billion DRAM market satisfies the needs of multiple industries with about 60% of the total chips being used by personal computer PC industry [5].

In general, the traditional memory technology can be classified into two main types – Volatile Memory and Non-Volatile Memory. Examples of volatile memory are the primary memory and the fast CPU cache memory. The primary memory is typically the DRAM and the fast CPU cache memory is typically the SRAM. SRAM is fast but energy-consuming and offers lower memory capacity per area unit than DRAM. Examples of non-volatile memory are flash

memory and ROM/PROM/EPROM/EEPROM memory family. Flash memories are sometimes used as secondary or primary computer memory whereas the ROM memories are typically used for firmware such as boot programs [6].

3.2 The cell operation

According to Mandelman's paper [7], typically a DRAM cell consists of a series of transistors, playing the role of transfer devices, and of storage devices (the capacitors). The word-line makes contact with the gate of the transfer device, and the bit-line contacts the source/drain of the transfer device; the end that is not connected to the storage capacitor. Data is written by turning on the transfer device by raising the word-line and writing a high or low voltage level onto the storage capacitor via the bit-line. Data is stored by turning off the transfer device by lowering the word-line, trapping the voltage/charge on the storage capacitor. Data is conventionally read by pre-charging the bit-line midway between the high and low levels, turning on the transfer device, and sensing the bit-line voltage change. The schematic below, Figure 1, shows the basic cell structure of a one transistor one capacitor (1T1C) DRAM cell.

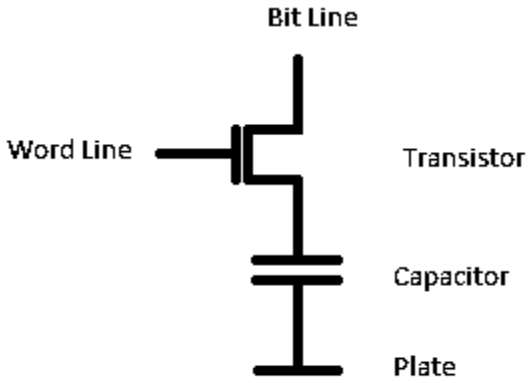

Figure 1: DRAM basic 1T1C [8]

3.3 The DRAM applications and Market trend

3.3.1 The DRAM applications

According to the literature, with each new DRAM product innovation the number of applications has increased tremendously. In the initial stages, applications for the DRAM have begun primarily with mainframe computers and have continued to expand as the types of computers, such as personal computers, have grown in number and these computers have been used in a wider variety of industrial and commercial settings. It is the technological improvements in the DRAM device which have caused the increase in the number of applications [9].

DRAMs have crucial role in computers, workstations, communication systems, and graphic subsystems. DRAM technology also drives the manufacturing infrastructure for the electronic industry. A rapid advancement in technology allowed an increase in bits/chip by a

factor of four every three years and a decline in cost/bit by roughly the same factor for 35 years. The experts expect this trend to continue as such for the next ten years. Three-dimensional cell structures in conjunction with lithography scaling and advances in doping, etching, planarization, and multilevel metallization help the reduction in cell size. These cell structures, and development/manufacturing techniques, have been successfully used for 4-Mbit to 256-Mbit DRAM generations and should be extendible at least to the 1 G-bit if not beyond [10]. Table 1 describes the various applications of the DRAM by generation.

Table 1: DRAM Applications

DRAM Device type	RAM Use	DRAM Device type	RAM Use
1 K	Mainframe	256 K / 1 Mb	Mainframe Minicomputer
4 K	Mainframe Mini-computer		Small business computer Portable computer
16 K	Mainframe Mini-computer Graphics		Personal computer Workstation CAD/CAM Robotics
54 K	Mainframe Mini-computer Personal computer Graphics		Graphics
		4Mb	Mainframe Minicomputer Home workstations Small business computer Portable computer Personal computer Laptop computer Workstation CAD/CAM/CIM Robotics HDTV Graphics

3.3.2 DRAM Current Market trend

The most significant growth driver in the DRAM industry market was the memory consumption in personal computing platforms. On the other hand, the definition of personal computing platforms has turned to be centered on mobile platforms as opposed to desktops and notebooks. Table 2 summarizes how mobile PC Shipment Growth changed in 2010 and 2011. Because NAND Flash is being used in place of DRAM for the system memory requirements, the

demand for DRAM memory has changed. The DRAM industry found growth in new, emerging areas like high-performance computing and high-performance networking [11].

Table 2: Mobile PC Shipment Growth [11]

Segment	2010	YoY	2011	YoY
NB (notebook included)	194M	21.30%	208M	7.30%
Netbook	33.2M	17%	25M	-24.60%
Tablet PC	15.7M	N/A	39.5M	152.40%
NB (notebook included) + Tablet PC	209.6M	31.20%	247.5M	18.10%

According to Table 3, average DRAM consumption per most devices is on a downward trend since 2006. But the shift in application, led by the growing demand in notebooks, HDTV and handsets barely offsets this reduction; it's not enough to fill the void completely. Table 3 summarizes the demand for DRAM based on the applications [4].

Table 3: Dram Demand by Application [4]

Applications	2006	2011	Difference (2011-2006)
Desktop	27%	18%	-9%
Notebook	15%	29%	14%
Server	8%	8%	0%
Upgrade Module	**25%**	**18%**	**-7%**
Graphics	5%	4%	-1%
Computer	**80%**	**77%**	**-3%**
DSC	2%	1%	-1%
Game Console	3%	1%	-2%
HDTV	2%	5%	3%
Handset	3%	6%	3%
Other	10%	10%	0%
Other Applications	**20%**	**23%**	**3%**

Figure 2 shows how revenue is divided among the memory segments and Figure 3 shows the trend for DRAM technology in data processing applications.

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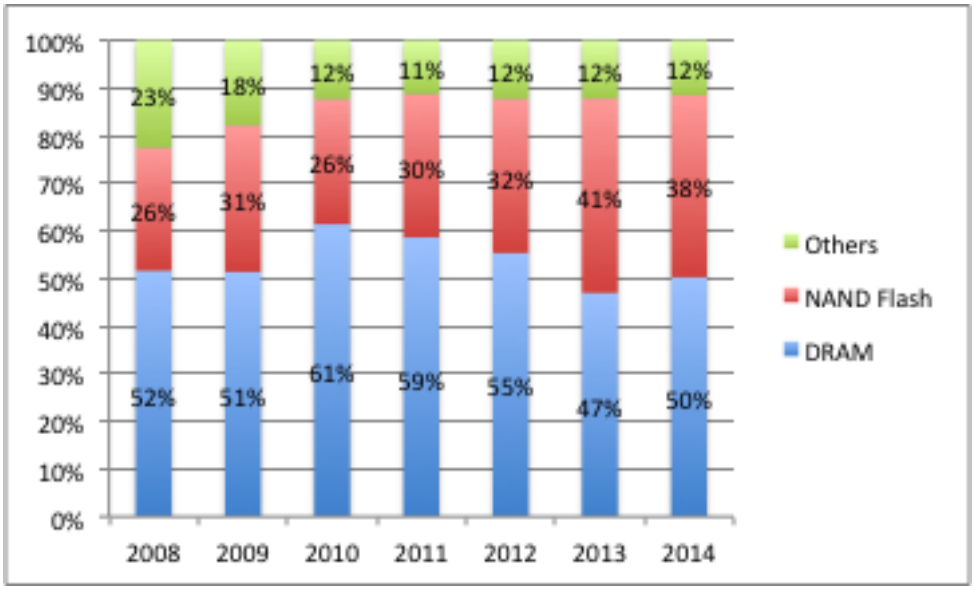


Figure 2: Revenue by Memory Segments [11]

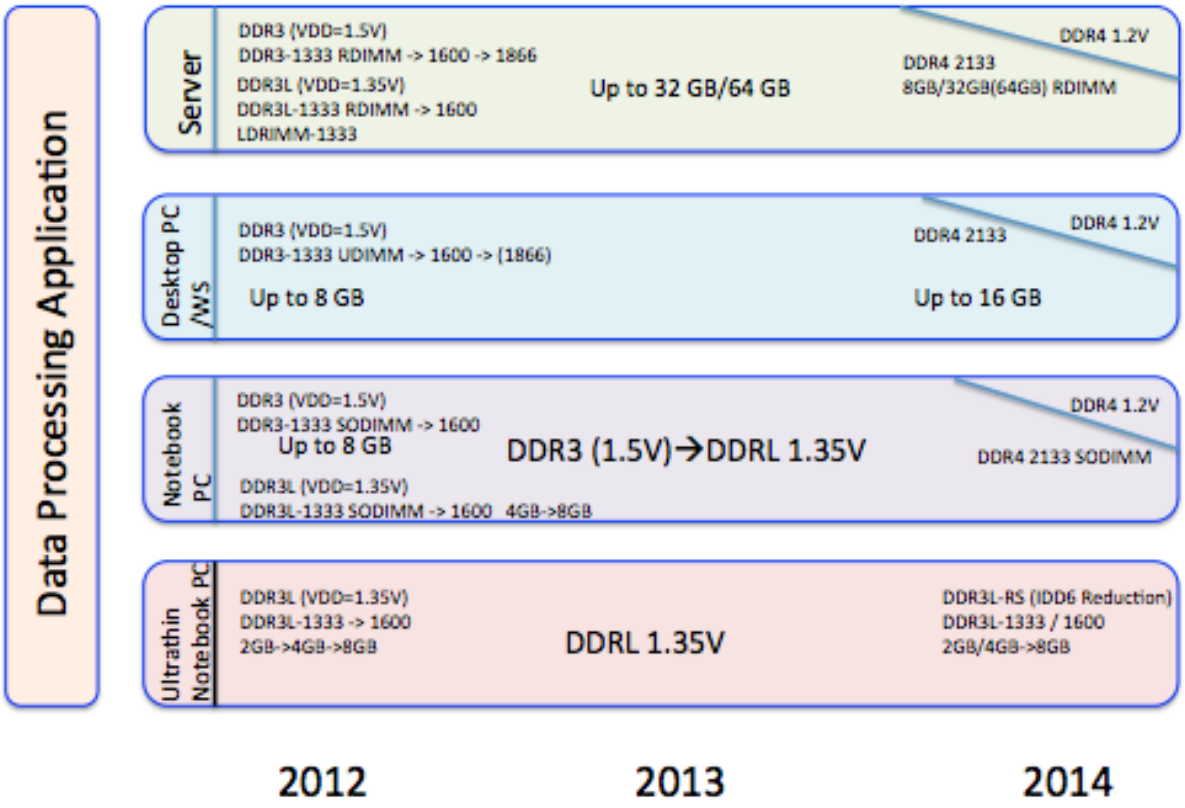


Figure 3: DRAM technology trend in data processing applications [11]

In the mobile memory space, the demands for higher performance, lower power DRAM solutions are resulting in the rapid introduction of new memory architectures. The mobile device market -including future phones, smartphones, and tablets- is continuing to generate its own set

of unique memory requirements, which are storage and speed [11]. Figure 4 shows the current trends in DRAM technology for mobile applications.

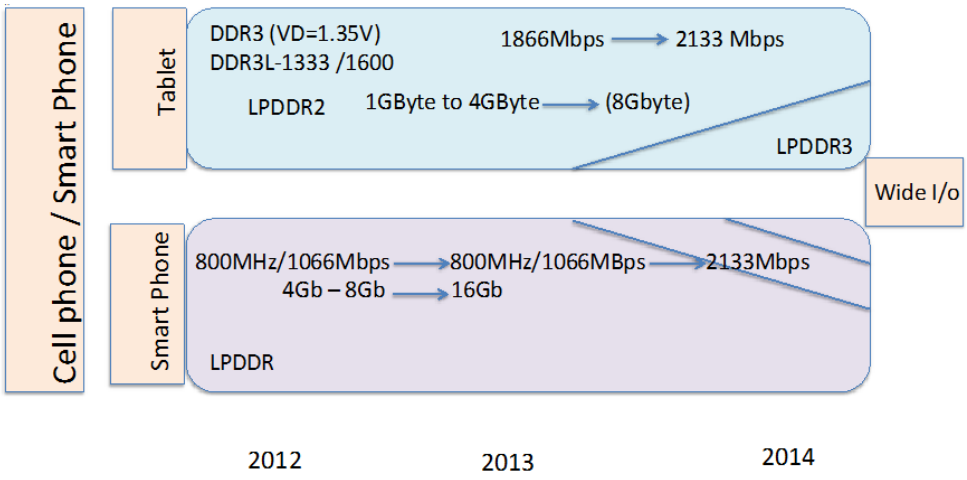


Figure 4: DRAM Technology trends in mobile applications [11]

3.4 Contributor to DRAM technology success

The learning from generation to generation, sometimes called the learning by doing plays a big role in the DRAM industry.

The fast pace at which the semiconductor industry reveals new products makes it a very interesting domain to observe, study and perform analysis. Alvarez [12] stated that the lessening of product cycles in the semiconductor industry leads to an important message that is, the quick and almost flawless introduction of new manufacturing processes are the key to successful competitive performance [12]. In this section of the paper the memory segment of the industry, and more specifically the DRAM part of it, is being looked at in order to understand the importance of learning from previous experiences (generations).

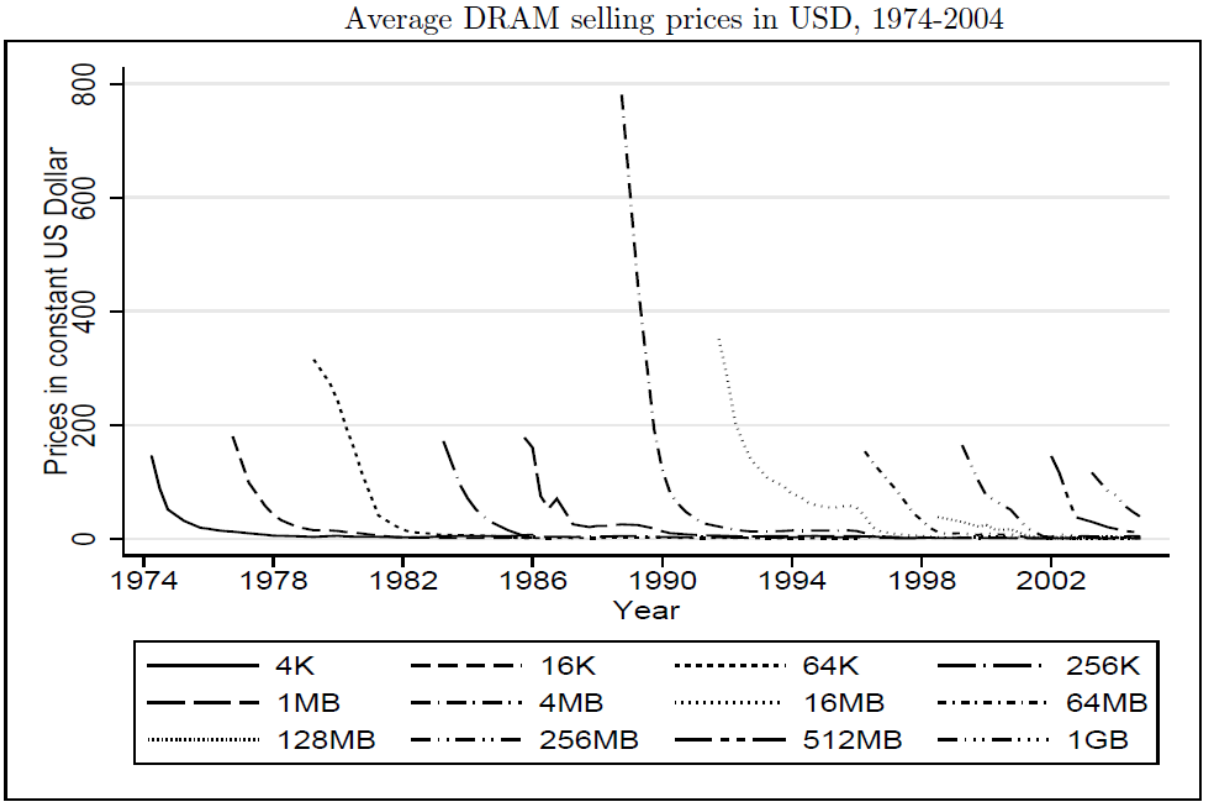
A model, of learning by doing, where engineering analysis of production data leads to improvements in yield was first introduced by Hatch & Reichelstein[1]. In the following year, Hatch & Mowery [13]improved the model by adding the factor of transferring new processes from a development environment to a mass production. The effect of the transfer on acquiring knowledge and yield was proven to be of a great impact [13]. The defect density parameter, a major contributor to yield, greatly benefited from the accumulation and transfer of learnt lessons that allowed a more controlled process and a significant reduction of random particles [13].

The DRAM sector is no exception to the rest of the semiconductor industry in the sense of ongoing needs to technological improvements in order to survive and advance. Indeed, smaller line widths and fewer particle counts are the greatest demands from the process. Being of a very

[1] Hatch, N. W. and Reichelstein S. 1997. Learning effects in semiconductor fabrication. Unpublished manuscript, University of Illinois at Urbana_Champaign.

simple design family, memory devices are nothing but repetitive identical cells in the die, engineering problem solving ought to be relatively fruitful in solving parametric yield issues and therefore the slope of the learning curve is steeper than other semiconductor devices [13]. To better benefit from the learning by doing concept, the DRAM industry/manufacturers stay away from a synchronized introduction of new product/generation and development process. Rather, the new process would be introduced and tested on the existing generation to allow better chances of learning due to the amount of collected data in a manufacturing environment [13].

Forgetting knowledge is a possible phenomenon over a long time period especially in a labor-intensive environment. This is not of any concern in the semiconductor industry due to its main characteristics of being capital-intensive and of short life cycles [14]. The importance and effect of the learning lessons expressed by the fine-tuning of the development processes, in addition to the mass production ability, are believed to be the main drivers behind the noticeable price decline over the DRAM generations as shown in the following graph[2] (Figure 5) [15].



Source: Gartner Inc. Prices are in constant US-$ as of 2000.

Figure 5: Average DRAM selling prices

[2] The graph 'Average DRAM selling prices in US,1974-2004' is adopted from 'figure 5' of R. Siebert and C. Zulehner.

4 DRAM Performance Parameters

The main parameters driving DRAM memory technologies for years have been: speed, density, and power consumption [16] [17].

- Speed:
  The speed of the memory determines the rate at which the CPU can process data. The higher the speed of the memory, the faster the system is able to read and write information from and to the memory. Data access of DRAM has historically been the bottleneck for many system applications, and DRAM architects have to come up with designs able to appropriately keep up with the CPU performance improvements. To benefit fully from the higher speed processors, the market shifts to the new families of faster DRAMs [5].
  Currently DRAM speed is designated by two factors: 1) the specific clock rate (in megahertz) that the memory's interface communicates to the processor, 2) the transfer rate or theoretical data bandwidth that the memory supports (megabytes transfers per second). DRAM speed and data rate have continuously improved with faster transistors and new interfaces (from Fast page mode to EDO, SDRAM, DDR, DDR2, DDR3…) [18].

- Density (Capacity):
  This parameter relates to the amount of bits of information that can be retained by the memory. As multitasking of applications increases, higher memory densities are greatly desired. Increasing DRAM density has a direct impact on performance as more data can be passed between the memory and the CPU. The key technology driver for higher memory densities is feature size down scaling (on going size reduction) [16].

- Power consumption:
  The need for low power consumption increases as more mobile devices predominate in the DRAM segment applications. As the cell size decreases, the resistance is reduced and less power is needed to operate the cells. This, in turn, means that less electrical current is needed for operation, and thus less time is needed to send the required amount of electrical charge into the system. To lower the power consumption in DRAM, lower operating voltage has been continuously implemented as seen from 3.3V ➔ 2.5V ➔ 1.8V ➔ 1.5V [18]. However, driving the power consumption lower and lower has a negative effect on the data retention time; an indispensable increase in the retention time will be a must at a certain point of the technology, which imposes challenges to the shrinking efforts of the DRAM technologists. Also as the feature size scales down (60 nm to 50nm and 40nm), difficulties to minimize the leakage currents at the storage node rise.

- Latency:
  Latency characterizes the time needed for a random read or write access. It specifically relates to the delay time between the moments a memory controller tells the memory module to access a particular location, and the moment the data from that given array location is available on the module's output pins. How low latency can be dropped and how high data-rate can be increased depends on the chip architecture, circuit design and

operation voltage, the supportive as well as the complementary technologies, and the various fields of application [19]. A point worth mentioning is that low latency and high performance impose cost overhead on the DRAM.

The different applications have specifically driven the improvements in the DRAM performance related to bandwidth, density, power consumption and data latency. High speed graphic applications drive the maximum data rate requirements. Server applications have pushed for increments in memory densities. Finally, the reduction of the required supply voltage comes mainly from requirements of reduction in power consumption of mobile and server applications [5]; As for the case of large data-center, a great portion of the power consumption is attributed to the DRAM refresh needs [19] , while in the case of mobile platforms the demand for longer hours of operation on a single charge drives the need for a well-management of the limited power budget offered by the battery capacities. In laptop and servers the latency and power consumption are parameters as important as compute performances.

In many cases these parameters are conflicting with each other and a solution can be found only if there is some trade-off, for example between the power consumption on one side and the performance on the other. These trade-offs will be mainly driven by the memory system (servers, laptops, mobile phones, etc.) requirements [19].

5 Threat of NAND and other emerging technologies

This section aims at introducing/defining the two main types of traditional flash memory technologies (NAND and NOR) along with the other emerging next generation memory technologies such as Memristor or Resistive RAM (RRAM), Magneto Resistive RAM (MRAM), PCRAM and Ferroelectric RAM (FeRAM). In addition, this section will also discuss the current trends in these technologies and how they pose threat to the DRAM technology.

Flash Memory – NAND and NOR

Flash memory is an electronic (i.e. no moving parts) non-volatile computer storage device that can be electrically erased and reprogrammed. There are two main types of flash memory, which are named after the NAND and NOR logic gates. The internal characteristics of the individual flash memory cells exhibit characteristics similar to those of the corresponding gates.

In addition to being non-volatile, flash memory offers fast read access times, as fast as dynamic RAM, although not as fast as static RAM or ROM. Its mechanical shock resistance helps explain its popularity over hard disks in portable devices; as does its high durability, being able to withstand high pressure, temperature, immersion in water, etc. [20].

Flash market is driven by cost per bit – scaling fueled by die cost reduction opportunities. Advanced lithography technology is a key factor in speed of NAND cost reduction. NAND floating gate scaling is expected to reach significant challenges at 1y /1z nm technology node [21].

The researchers have concluded that even at today's prices, a dollar's worth of NAND flash improves PC performance more than adding a dollar's worth of DRAM. They propose that "an appropriate balance of NAND, DRAM, and an HDD yields superior performance per dollar to a simple DRAM/HDD system" [22]. But NAND-flash has generally been considered to be too slow for use as a main memory technology. Results indicate that using flash, along with DRAM, to build a hybrid memory system may be a compelling design point for future memory systems and hence hybrid memory systems need more investigation as a cost effective way to build large memory systems of the future [23].

Emerging next generation Memory Technologies

Memories are getting increasing importance since they are becoming fundamental in the definition of the electronic system. Presently the industry standard technologies are still DRAM and Flash that have been able to guarantee the cost sustainability thanks to the continuous scaling. The NAND/DRAM miniaturization is becoming increasingly difficult and moreover new applications are requiring higher memory density and better performances. Therefore there are good opportunities for the alternative memory technologies to enter into the market and replace/displace the standard ones [19]. The emerging nonvolatile memory technologies are gaining significant attentions from semiconductor in recent years. Multiple promising candidates, such as phase change memory, magnetic memory, resistive memory, and memristor, have gained substantial attentions and are being actively pursued by industry [24].

Memristors

Memristors are basically a fourth class of electrical circuit, joining the resistor, the capacitor, and the inductor, that exhibit their unique properties primarily at the nanoscale [25]. Until recently, when HP Labs under Stanley Williams developed the first stable prototype, memristance as a property of a known material was nearly nonexistent. Currently IBM, Hewlett Packard, HRL, Samsung and many other research labs seem to be hovering around the titanium dioxide memristor, but there are quite a few other types of memristors (such as polymeric memristors, ferroelectric memristors and spin memristive systems) with vectors of inquiry [25]. Memristors are expected to be the future key market players once they prove commercially successful.

Magneto Resistive RAM (MRAM)

Magnetoresistive random-access memory (MRAM) is a non-volatile random-access memory technology that has been under development since the 1990s. Continued increases in density of existing memory technologies – notably flash RAM and DRAM – kept it in a niche role in the market, but its proponents believe that the advantages are so overwhelming that magnetoresistive RAM will eventually become dominant for all types of memory, becoming a universal memory [26]. MRAM is fast, high-density and non-volatile and has the potential to replace all kinds of memories used today in a single chip [27].

Phase Change Memory (PCRAM)

Phase-change memory (also known as PCM, PCME, PRAM, PCRAM, Ovonic Unified Memory, Chalcogenide RAM and C-RAM) is a type of non-volatile random-access memory. PRAMs exploit the unique behavior of chalcogenide glass. Newer PCM technology has been trending in a couple different directions. Some groups have been directing a lot of research towards attempting to find viable material alternatives to $Ge_2Sb_2Te_5$ (GST), with mixed success, while others have developed the idea of using a GeTe - Sb_2Te_3 superlattice in order to achieve non thermal phase changes by simply changing the coordination state of the Germanium atoms with a laser pulse, and this new Interfacial phase change memory (IPCM) has had many successes and continues to be the site of much active research [28]. In February 2012, Samsung has presented 20nm 1.8V 8Gb PRAM [29] and in July 2012, Micron has announced the availability of Phase-Change Memory for mobile devices - the first PRAM solution in volume production [30]. So, PCM is expected to emerge further in the near future.

Ferroelectric RAM (FeRAM)

Ferroelectric RAM (FeRAM, F-RAM or FRAM) is a random-access memory similar in construction to DRAM but uses a ferroelectric layer instead of a dielectric layer to achieve non-volatility. FeRAM is one of a growing number of alternative non-volatile random-access memory technologies that offer the same functionality as flash memory [31].

Ferroelectric random access memory (FeRAM) has been intensively studied because of its superior performance as a non-volatile memory. Lower power consumption, faster read/write cycle and longer endurance compared to a conventional EEPROM are suitable for various non-volatile applications. In addition, the memory cell structure similar to dynamic random access memory (DRAM) indicates a high potential to realize large scale FeRAM with 1G-bit or higher density. FeRAM process technology is basically compatible with that of logic devices. This feature enables FeRAM to extend the application area from pure memory to embedded memory. Although FeRAM is recognized as a universal memory because of such superiority, further innovations are needed to realize the replacement of all memories to FeRAM [32].

6 Technologies affecting the DRAM industry

6.1 Lithography

Lithography[3], from a semiconductor industry point of view where it is called photolithography or simplified to the term Litho, is the fine art that allows the transferring of electronic circuitry images onto the surface of a treated wafer at a specific reduction rate. The art started in the early 1960s and went through tremendous deal of technological improvements to reach todays ability of printing (transferring the image from a mask) on a wafer at a Nano scale.

Photolithography plays a major contributor role in the DRAM industry. In some of the reviewed literature, photolithography has been considered as the core technology of DRAM and accounting for 20% of the fixed cost [4]. In addition to other technologies, the advanced lithography made it possible for the DRAM manufacturers to produce larger units in terms of

[3] http://en.wikipedia.org/wiki/Photolithography. Accessed on 2/18/2013

memory storage capacity but smaller in terms of physical dimensions. By the end of 2012, according to the International Technology Roadmap for Semiconductors ITRS, the industry was supposed to decide on which lithography method to be utilized for the 22 nm half-pitch DRAM [15]. The decision has not been made yet and that is expected due to the fact that the current ArF (Argon Fluoride LASER 193 nm) immersion lithography is not capable of being extended well below 40 nm half-pitch [33]. The main point to focus on is not the ability to print smaller, but the ability to deliver better performing DRAM at a cheaper cost per transistor [15]. For the time being, the potential solution to the lithography tense moments are displayed in the following graph[4] (Figure 6) where the descending listing order represents the probability of dominance of the specific technology [34]. The suggested solutions are proposed with the assumption that the required infrastructure, from exposure tools to appropriate photoresist to the delicate masks and the necessary metrology tools, be in place at the time of implementation. Experience has proven that the roadmap has been always overachieved and ahead of estimated dates by the industry [15].

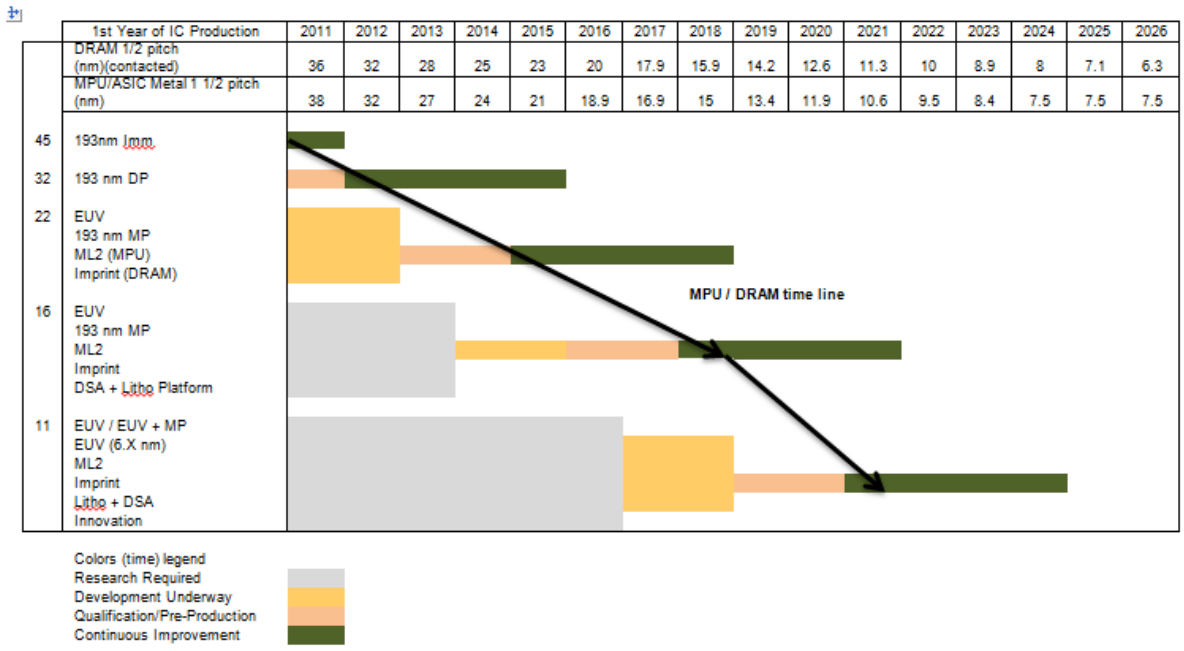


Figure 6: Lithography Exposure Tool Potential Solutions for MPU and DRAM Devices

From Figure 6, it could be concluded that for the time being the leading lithography technology is the 193 nm immersion with double print followed by the multiple print (193nm DP & MP). The most probable futuristic technology that would enable patterning for 22 nm half-pitch and below is the Extreme Ultraviolet Lithography (EUVL). Finally, the Nano-Imprint Lithography (NIL) that is not currently driven by the semiconductor industry might be an option if the surrounding difficulties and uncertainties find the correct resolving answers. Those were

[4] The graph is adopted from the ITRS 2011 Edition, Lithography

the short term forecasted techniques envisioned and entertained by the experts in the lithography domain.

An important note to mention at this point and to possibly expand at a later stage of the paper is that, the DRAM device improvement does not depend solely on lithography. Some of the main DRAM performance specifications, such as speed & power consumption, heavily depend on the capacitance of its storage capacitor that is expressed as $C_s = {}_iA/T_i$ where ${}_i A$, T_i are permittivity of storage insulator, area of capacitor electrode, and insulator thickness respectively [3]. A careful look at the capacitance formula should lead to the following observation; the continuous shrinking of the DRAM cell size will automatically shrink and reduce the area of capacitor electrode (A in the formula) which in turn leads to a lesser C_s capacitance value, hence the need to look for other technological innovations to complement the lithography efforts in maintaining the DRAM on the far future radar map.

6.2 The material science frontier

As discussed in the previous sections, the DRAM industry, or the entire semiconductor industry to be more precise, has been able to faithfully fulfill the rules of Moore's by driving the lithography technology close to its imaginary limits. Therefore, with the shrinkage of the semiconductor geometry and line width, the ability of building higher density DRAM on the same die landscape had not been a threatening challenge. Recalling the capacitance formula from the previous section ($C_s = {}_iA/T_i$) strengthens our belief that, the main concern of DRAM authorities is the fight against the natural limit of physics. Large capacity and low leakage at the storage node are the differentiator design factors and the main controllers of the parameters that describe the DRAM performance [35]. Therefore, as the cell design keeps on shrinking down the active capacitor area will be reduced and leads to two major setbacks, the decrease in the cell capacitor storage capacity and the inescapable increase in the leakage current due to the tunneling effect phenomenon and consequently an increase in the power dissipation/consumption [36]. A feasible solution would be a new material for the capacitor insulator with a high permittivity (high dielectric constant, 'High-K material') larger than the conventional silicon oxide (SiO_2).

In the recent years, efforts were focused on investigating a wide range of high-k materials to be applied on the silicon (Si) substrates. The list included the following binary oxides: HfO_2, ZrO_2, TiO_2, Al_2O_3, Y_2O_3, etc., as well as the following ternary oxides: silicates ($MSiO_x$), aluminates ($MAlO_x$), hafnates ($MHfO_x$), etc., where the M means Metal [37]. The Hf –related high-k materials such as the HfO_2, Hf silicates (HfSiO), and HfSiON are viewed as the most promising materials suitable to replace the traditional SiO_2 [37].

7 Research Methodology

This study uses Technology Forecasting using Data Envelopment Analysis (TFDEA) as the methodology to forecast the future of DRAM industry. TFDEA is an extension of DEA in the field of technology forecasting which has been introduced and developed at Portland State University by Anderson *et al*. It has been successfully applied in prior technology forecasting studies such as fighter jets, microprocessors, USB drives, computer display projectors and

wireless technologies to evaluate a technology's historical stages along with the State-of-the-art so that characteristics of the technology's future can be identified [38] [39]. Since TFDEA is explained extensively in the literature, this paper will not attempt to detail the methodology. Interested readers can look for further detailed information from [40]. This paper aims to apply TFDEA in the technology forecasting for the DRAM industry for the first time.

7.1 Model parameters

From the literature review of the DRAM parameters, one can understand that the driving parameters cannot be generalized across the different applications of the DRAM. For instance, even though Power consumption and Latency are the two key general parameters for the DRAMs, power consumption has higher consideration in the mobile DRAMs compared to latency whereas latency is given more consideration in the computing DRAMs compared to power consumption. But on the other hand, any DRAM is expected to deliver exceptional performance and so the output for that matter does not vary based on the application area of the DRAM. There is no effective way to classify parameters based on their levels of importance in TFDEA. So, this study uses a TFDEA model with CAS latency and voltage (in place of power consumption) as inputs and transfer rate and density as outputs for both computing and mobile DRAMs. Figure 7 describes the TFDEA model for the DRAM. Given the trends that mobile DRAMs have prevalent growth when compared to Computing DRAMs, this study intends to analyze both segments separately.

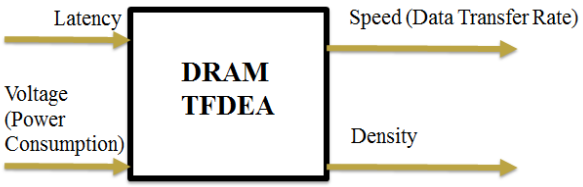


Figure 7: TFDEA Model for DRAM

When Density was included as one of the output parameters the results of the model yielded to RoC of about 50% for both Computing and Mobile DRAMs. These results implied that for every two years speed and density would double, which is not the case for speed. Only density doubles for every DRAM generation as DRAM capacity has showed the trend of changing from 64 Mbit to 128 Mbit to 256 Mbit etc. So, in order to have a better idea about the improvements in the Transfer rate (speed), the density parameter was excluded from the TFDEA model for DRAM as shown Figure 8.

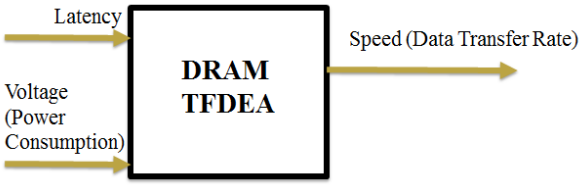


Figure 8: Updated TFDEA Model for DRAM

7.2 Data Collection

The main source of data collection for this study is the internet especially from the manufacturers' website such as Samsung and Micron. The product selection guides from Samsung for every year in mobile DRAMs contributed significantly for the mobile DRAM data collection.

8 TFDEA Model Implementation

This study uses the TFDEA software developed by Lim and Anderson [41].

8.1 Input/output Orientation

In order to determine the efficient (i.e. 'best practice') frontier using DEA, one can choose between DEA input-oriented and output-oriented models, based on the objective of the technology under study. An input-oriented model is used when the target for the product under analysis is to minimize its input for a given output. An output-oriented model is used when the scope is output maximization for a given input. In the case of the DRAM industry, since the focus is to maximize performance for every generation which in turn impacts the transfer rate, an output-orientated model is used in this study.

8.2 Frontier Year

The general rule in forecasting by TFDEA is that the number of DMUs is suggested to be at least one third of total number of input and output parameters [40]. Figure 9 shows the number of DMUs in the computing DRAM dataset and Figure 10 shows the number of DMUs in the mobile DRAM dataset respectively.

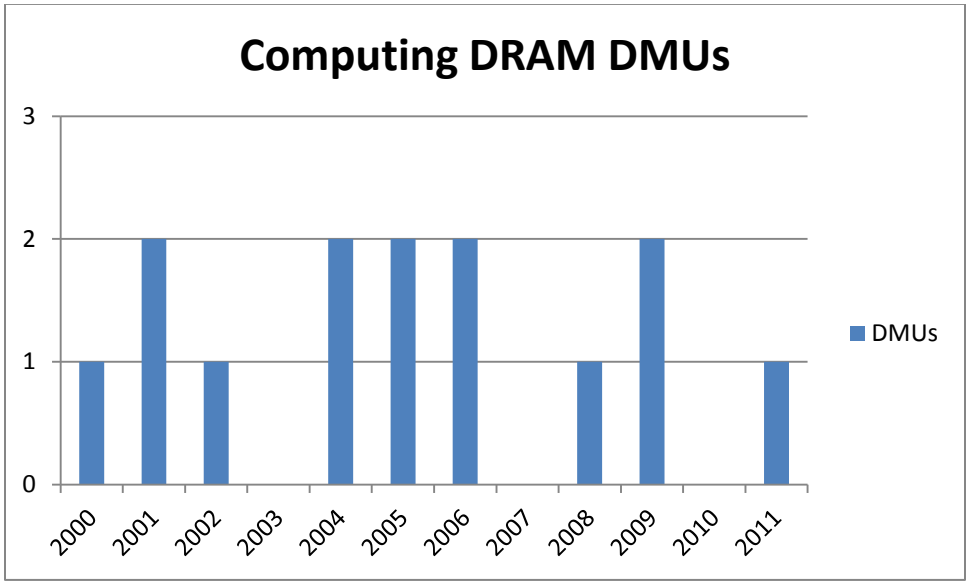


Figure 9: DMU count per year for the computing DRAMs

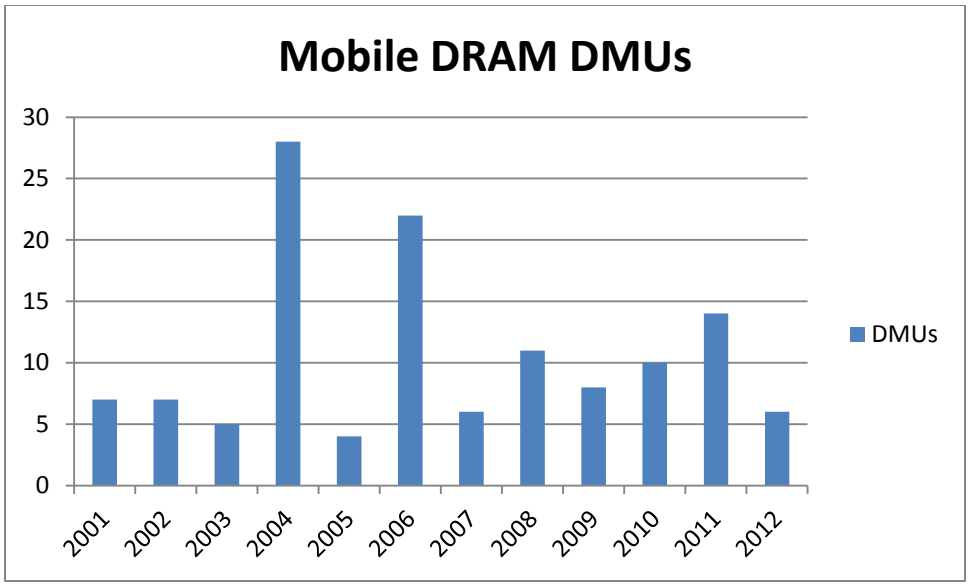


Figure 10: DMU count per year for the mobile DRAMs

A proper frontier year would be the one that is recent enough so that the rate of change calculated by TFDEA includes the recent technological advances. There should also be enough number of DMUs after the year of frontier to verify the validity of the model's forecast. So, in order to backtest the model, frontier year 2007 is used for both computing and mobile DRAMs in this study.

9 Discussion of Results

The created models were evaluated via back-testing which was performed against historical data. The historical data was divided into two sets for both technologies:

- Computing DRAMs: learning period (from 2000 to 2007) and the validation period (from 2008 to 2011).
- Mobile DRAMs: learning period (from 2001 to 2007) and the validation period (from 2008 to 2012).

Models settings were chosen after multiple testing to be as following that deliver the best results:

- Output Orientation;
- Variable Returns to Scale for Computing DRAMs; Constant Returns to Scale for Mobile DRAMs;
- Frontier years: 2007 for both computing and mobile DRAMs.

Then the model results were compared against the actual historical data for this period. Both the RoC (Rate of Change) as well as MAD (Median Absolute Deviation) value was calculated.

Table 4: RoC and MAD values for the models

Model	RoC	MAD
Computing DRAM	1.265198	0.976156
Mobile DRAM	1.337866	0.4738939

Figure 11 and Figure 12 show the forecasted date vs. actual release date charts for both computing and mobile DRAMs. The red line on the graphs represents the ideal forecast by the model, i.e. The actual release year matches with the model prediction. The area above the red line shows the products that were produced earlier than the model predicted, below the red line shows the ones produced after the forecast prediction.

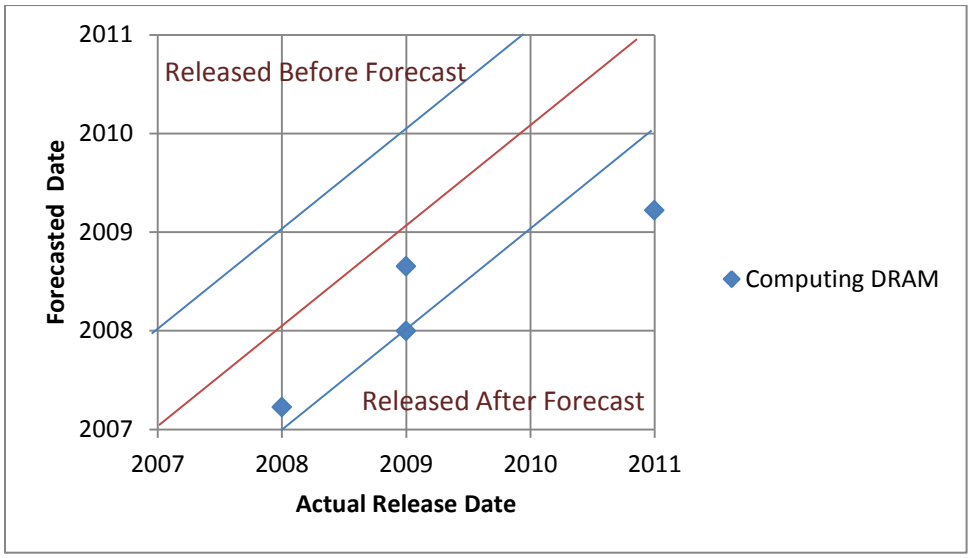


Figure 11: Forecasted Date vs. Actual Release Date for Computing DRAMs

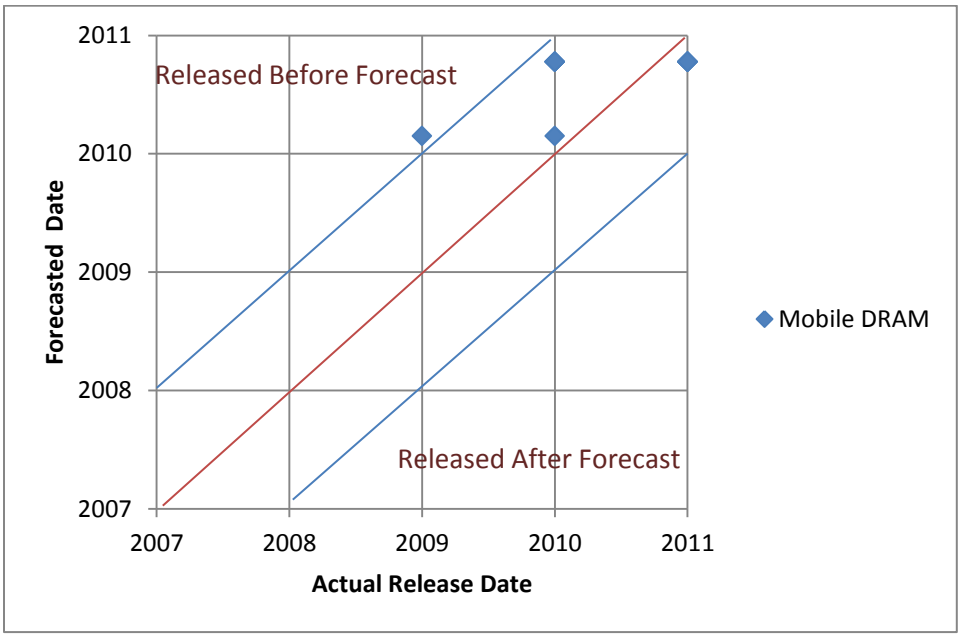


Figure 12: Forecasted Date vs. Actual Release Date for Mobile DRAMs

From Figure 11 and Figure 12 it can be noticed that for the Computing dataset, the actual DRAMs were released after the prediction, while in the case of the mobile dataset, the actual DRAMs were released before the forecast. These results imply that there has been a deceleration in the computing DRAM, and acceleration in the Mobile DRAM, which can be attributed to prevalent growth of mobile applications. Figure 13 shows the RoC trends for the computing DRAMs for the different frontier years.

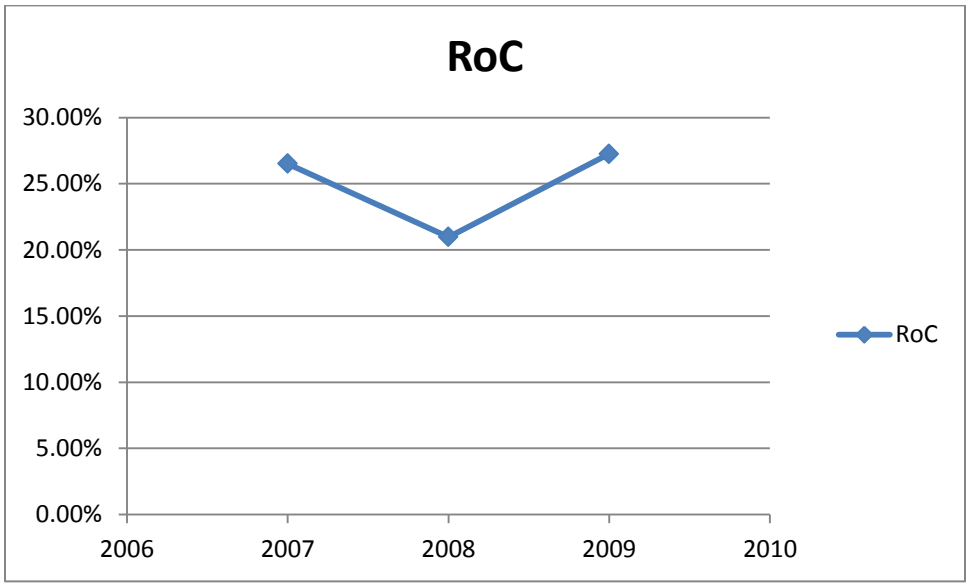


Figure 13: RoC Trend for Computing DRAMs

10 Implications

The results obtained indicate that there have been continuous improvements in the performance characteristics of both the computing and mobile DRAMs. Since this is an output oriented model, it implies that the data rate is changing at a RoC of 26.52±2.81 for the computing DRAM and 33.79±4.67 for the mobile DRAM respectively with a confidence interval of 95% (Table 5 and Table 6.)

Table 5: Computing DRAM - RoC and SD values for Frontier year 2007

Rate of Change	1.265198
Standard Deviation	0.02872
95% Confidence Interval	± 0.028145

Table 6: Mobile DRAM - RoC and SD values for Frontier year 2007

Rate of Change	1.337866
Standard Deviation	0.09243

95% Confidence Interval	± 0.046775

The above results show that the data rates are expected to double every 3 to 4 years which is in agreement with the ITRS projections for DRAM data rates for 2009 including DDR2, DDR3 and DDR4 families [42] [43].

11 Conclusions

The literature review revealed a great deal of information about the DRAM products, applications, markets, and technologies as well. Being part of the semiconductor industry, the DRAM sector had and still follows a fast trend of innovation and development. Moore's law application had survived many obstacles and was able to overcome many threats of being proven absolute. Yet, nature and physics pose unsurpassable limits, in the DRAM case the capacitor active areas size, that scientists and technologists understand very well and are taking all possible measures to maintain Moore's law alive at least at one of the DRAM parameter which in turn contributes to the overall performance improvement slope.

An interesting point to mention is that despite the general similarity between the DRAM and the microprocessor development and fabrication technologies, the difference in application purposes and the final market segments prevented a 'copy exactly' of what is happening in one technology into the other one. Currently the DRAM devices are manufactured on DRAM-optimized technologies while the microprocessor units (MPUs) are generally fabricated on logic-optimized technologies [8]. The inability of switching technology is not due to pure technical limitations; Functional devices could be manufactured either way, but economic factors and performance preferences dictate the use of a specific technology. The DRAM has become a commodity product while the MPU remained a specialized device therefore the DRAM manufacturing cost sensitivity drew the line of which technology to be used [8].

Because the Internet diffuses very rapidly, the growth in high-speed communications and cloud computing are the new demands on computer data center infrastructures. The growing demands are resulting in new memory technologies and better performance requirements. Virtualization of data center services is driving the expansion of these centers, which places increasing demands on cooling, back-up, and high-speed data transmission. To meet these demands, more memory types (like DDR4) are required with higher speed, higher density, and lower power consumption. Beyond DDR4, new technologies like High-Bandwidth Memory (HBM), Hybrid Memory Cube (HMC), and Wide I/O II are being developed at an aggressive pace to provide next-generation solutions.

We can conclude that DRAM can continue its current trend in the short and medium future terms as long as the improvements in the supportive technologies such as lithography and others contribute to make these projections a reality. Also, it should be noted that if the physical limitations are not overcome in the DRAM industry, there are other prospective emerging technologies in the long run that could compete with DRAM in order to deliver better results.

12 Limitations of the study and Future work

As mentioned previously, the datasets used in this study are collected from the manufacturers' websites and not from any central repository or database. So chances of the data being slightly off exist in real-time scenario. The future work could include revisiting both the computing and mobile datasets and calculating the rate of change values.

Due to time limitations, this study did not separate the server and PC markets separately; instead, combines both the data values as a single computing dataset. Future work could separate the computing dataset into PC and server datasets separately and analyze results.

This study has used TFDEA alone as the key methodology to study the future of DRAMs. Future work could include other technology forecasting techniques such as regression, TDE (Technology Development Envelope) etc. and results could be analyzed.

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Results

Run by TFDEA add-in ver 2.2

Frontier Type	Orientation	2nd Goal	Return to Scale	Avg RoC	Frontier Year	MAD
Dynamic	OO	Max	VRS	1.265198	2007	0.976156

Input(s)	Output(s)	SOA products at Release	SOA products on Frontier	RoC contributors	Release before forecast	Release after forecast
2	1	8	1	4	0	4

DMU	Name	Date	Efficiency_R	Efficiency_F	Effective Date	Rate of Change	Forecasted Date
1	PC-1600 DDR SDRAM	2000	1	5	2006.000000	1.307660	-
2	PC-2100 DDR SDRAM	2001	1.250351617	3.750586029	2006.000000	-	-
3	PC-2700 DDR SDRAM	2001	1	2.999625047	2006.000000	1.245700	-
4	PC-3200 DDR SDRAM	2002	1	2.5	2006.000000	1.257433	-
5	PC2-4200 DDR2 SDRAM	2004	1	1.875293015	2006.000000	-	-
6	PC2-3200 DDR2 SDRAM	2004	1.333125	2.5	2006.000000	-	-
7	PC2-5300 DDR2 SDRAM	2005	1.200075005	1.500093756	2006.000000	-	-
8	PC2-6400 DDR2 SDRAM	2005	1	1.25	2006.000000	1.250000	-
9	PC3-8500 DDR3 SDRAM	2006	1	1	2006.000000	-	-
10	PC3-6400	2006	1.25	1.25	2006.000000	-	-
11	PC3-10600 DDR3 SDRAM	2008	1	0.749976563	2006.000000	-	2007.223120
12	PC3-12800 DDR3 SDRAM	2009	1.166640625	0.625	2006.000000	-	2007.998069
13	PC3-14900 DDR3 SDRAM	2009	1	0.535726244	2006.000000	-	2008.653296
14	PC3-17000 DDR3 SDRAM	2011	1	0.468768311	2006.000000	-	2009.220890

Results

Run by TFDEA add-in ver 2.2

Frontier Type	Orientation	2nd Goal	Return to Scale	Avg RoC	Frontier Year	MAD
Dynamic	OO	Max	CRS	1.337866	2007	0.473894

Input(s)	Output(s)	SOA products at Release	SOA products on Frontier	RoC contributors	Release before forecast	Release after forecast
2	1	32	12	15	9	10

DMU	Name	Date	Efficiency_R	Efficiency_F	Effective Date	Rate of Change	Forecasted Date
1	MT48LC4M32LFB5-8	2001	1.144	3.2	2007.000000	-	-
2	MT48LC8M16LFB4-75M	2001	1.07518797	3.007518797	2007.000000	-	-
3	K4S643234E	2001	1	2.797202797	2007.000000	1.187009	-
4	K4S643233E	2001	1	2.797202797	2007.000000	1.187009	-
5	K4S641633F	2001	1.07518797	3.007518797	2007.000000	-	-
6	K4S281633D	2001	1.07518797	3.007518797	2007.000000	-	-
7	K4S28163LD	2001	1.07518797	3.007518797	2007.000000	-	-
8	K4S64323LF	2002	1.07518797	3.007518797	2007.000000	-	-
9	K4S643233F	2002	1.07518797	3.007518797	2007.000000	-	-
10	K4S561633C	2002	1.07518797	3.007518797	2007.000000	-	-
11	K4S56163LC	2002	1.07518797	3.007518797	2007.000000	-	-
12	K4M563233D	2002	1.144	3.2	2007.000000	-	-
13	K4M28163PD	2002	1	3.80952381	2007.000000	1.306695	-
14	K4S511633C	2002	1.144	3.2	2007.000000	-	-
15	K4M28163LF	2003	1.248120301	3.007518797	2007.000000	-	-
16	K4M281633F	2003	1.248120301	3.007518797	2007.000000	-	-
17	K4S28323LE	2003	1	2.409638554	2007.000000	1.245914	-
18	K4S283233E	2003	1	2.409638554	2007.000000	1.245914	-
19	K4M64163PH	2003	1	3.007518797	2007.000000	1.316898	-
20	K4S64323LH	2004	1	2.409638554	2007.000000	1.340656	-
21	K4S643233H	2004	1.003012048	2.409638554	2007.000000	-	-
22	K4S64163LH	2004	1.248120301	3.007518797	2007.000000	-	-
23	K4S641633H	2004	1.251879699	3.007518797	2007.000000	-	-
24	K4M51163LE	2004	1.328	3.2	2007.000000	-	-
25	K4M51153LE	2004	1.328	3.2	2007.000000	-	-
26	K4M28163PF	2004	1	3.007518797	2007.000000	1.443453	-
27	K4S56323PF	2004	1	3.007518797	2007.000000	1.443453	-
28	K4S56323LF	2004	1	2.409638554	2007.000000	1.340656	-
29	K4S563233F	2004	1.003012048	2.409638554	2007.000000	-	-
30	K4S56163PF	2004	1	3.007518797	2007.000000	1.443453	-
31	K4S56163LF	2004	1.248120301	3.007518797	2007.000000	-	-
32	K4S561633F	2004	1.251879699	3.007518797	2007.000000	-	-
33	K4S51323PF	2004	1	3.007518797	2007.000000	1.443453	-
34	K4S51323LF	2004	1.248120301	3.007518797	2007.000000	-	-
35	K4S513233F	2004	1.251879699	3.007518797	2007.000000	-	-
36	K4S51163PF	2004	1	3.007518797	2007.000000	1.443453	-
37	K4S51163LF	2004	1.248120301	3.007518797	2007.000000	-	-
38	K4S511633F	2004	1.251879699	3.007518797	2007.000000	-	-
39	K4S51153LF	2004	1.248120301	3.007518797	2007.000000	-	-
40	K4S511533F	2004	1.251879699	3.007518797	2007.000000	-	-
41	K4S28323LF	2004	1	2.409638554	2007.000000	1.340656	-
42	K4S283233F	2004	1.003012048	2.409638554	2007.000000	-	-
43	K4M56323LE	2004	1.328	3.2	2007.000000	-	-
44	K4M563233E	2004	1.251879699	3.007518797	2007.000000	-	-

45	K4M56163PE	2004	1	2.402402402	2007.000000	1.339312	-
46	K4M51323LE	2004	1.328	3.2	2007.000000	-	-
47	K4M513233E	2004	1.251879699	3.007518797	2007.000000	-	-
48	MT46H16M16LFBF-6	2005	1.201201201	1.201201201	2007.000000	-	-
49	MT46H16M16LFBF-5 IT	2005	1	1	2007.000000	-	-
50	K4M64163PK	2005	3.007518797	3.007518797	2007.000000	-	-
51	K4M28323PH	2005	3.007518797	3.007518797	2007.000000	-	-
52	MT48H4M16LFB4-8	2006	3.2	3.2	2007.000000	-	-
53	MT48H8M16LFB4-75	2006	3.007518797	3.007518797	2007.000000	-	-
54	MT48H16M16LFBF-75	2006	3.007518797	3.007518797	2007.000000	-	-
55	MT48H4M16LFB4-75	2006	3.007518797	3.007518797	2007.000000	-	-
56	K4M641633K	2006	3.007518797	3.007518797	2007.000000	-	-
57	K4M64163LK	2006	3.007518797	3.007518797	2007.000000	-	-
58	K4M283233H	2006	2.409638554	2.409638554	2007.000000	-	-
59	K4M28323LH	2006	2.409638554	2.409638554	2007.000000	-	-
60	K4M281633H	2006	3.007518797	3.007518797	2007.000000	-	-
61	K4M28163PH	2006	3.007518797	3.007518797	2007.000000	-	-
62	K4M563233G	2006	2.409638554	2.409638554	2007.000000	-	-
63	K4M56323LG	2006	2.409638554	2.409638554	2007.000000	-	-
64	K4M56323PG	2006	3.007518797	3.007518797	2007.000000	-	-
65	K4M561633G	2006	3.007518797	3.007518797	2007.000000	-	-
66	K4M56163LG	2006	3.007518797	3.007518797	2007.000000	-	-
67	K4M56163PG	2006	3.007518797	3.007518797	2007.000000	-	-
68	K4M513233C	2006	3.007518797	3.007518797	2007.000000	-	-
69	K4M51323LC	2006	3.007518797	3.007518797	2007.000000	-	-
70	K4M51323PC	2006	3.007518797	3.007518797	2007.000000	-	-
71	K4M511633C	2006	3.007518797	3.007518797	2007.000000	-	-
72	K4M51163LC	2006	3.007518797	3.007518797	2007.000000	-	-
73	K4M51163PC	2006	3.007518797	3.007518797	2007.000000	-	-
74	MT46H32M32LFCM-75	2007	1.503759398	1.503759398	2007.000000	-	-
75	MT46H4M32LFB5-6	2007	1.201201201	1.201201201	2007.000000	-	-
76	MT46H32M32LFCM-6	2007	1.201201201	1.201201201	2007.000000	-	-
77	MT46H64M16LFCK-6	2007	1.201201201	1.201201201	2007.000000	-	-
78	MT46H64M32L2KQ-6 IT	2007	1.201201201	1.201201201	2007.000000	-	-
79	MT46H32M32LFCG-5 IT	2007	1	1	2007.000000	-	-
80	MT46H16M32LFCG-6	2008	1.201201201	1.201201201	2007.000000	-	-
81	MT46H8M16LFBF-5 IT	2008	1	1	2007.000000	-	-
82	MT46H64M32L2CG-5 IT	2008	1	1	2007.000000	-	-
83	MT48H4M32LFB5-75	2008	2.506265664	2.506265664	2007.000000	-	-
84	MT48H8M16LFB4-6 IT	2008	2.395209581	2.395209581	2007.000000	-	-
85	MT48H16M16LFBF-6	2008	2.395209581	2.395209581	2007.000000	-	-
86	K4M56163PI	2008	3.007518797	3.007518797	2007.000000	-	-
87	K4M56323PI	2008	2.409638554	2.409638554	2007.000000	-	-

88	K4X56323PI	2008	1.503759398	1.503759398	2007.000000	-	-
89	K4X51323PE	2008	1.503759398	1.503759398	2007.000000	-	-
90	K4X1G163PC	2008	1.503759398	1.503759398	2007.000000	-	-
91	MT46H128M32L2KQ-6 IT	2009	1.201801802	1.201201201	2007.000000	-	-
92	MT46H128M32L2KQ-5 IT	2009	1.0005	1	2007.000000	-	-
93	MT42L64M32D1KL-3 IT	2009	1	0.3998001	2007.000000	-	2010.149665
94	K4M51163PG	2009	2.410843373	2.409638554	2007.000000	-	-
95	K4M51323PG	2009	2.410843373	2.409638554	2007.000000	-	-
96	K4X56323PI	2009	1.504511278	1.503759398	2007.000000	-	-
97	K4X1G163PC	2009	1.504511278	1.503759398	2007.000000	-	-
98	K4X2G303PD	2009	1.504511278	1.503759398	2007.000000	-	-
99	MT42L128M32D2KL-3 IT	2010	1.1994003	0.3998001	2007.000000	-	2010.149665
100	MT42L128M16D1KL-25 IT	2010	1	0.333333333	2007.000000	-	2010.774320
101	MT48H32M32LFB5-75 IT	2010	3.609022556	3.007518797	2007.000000	-	-
102	MT48H32M32LFB5-6 IT	2010	2.874251497	2.395209581	2007.000000	-	-
103	K4X2G163PC	2010	1.2	1	2007.000000	-	-
104	K4X2G323PC	2010	1.2	1	2007.000000	-	-
105	K4X4G303PB	2010	1.2	1	2007.000000	-	-
106	K4P1G324EE	2010	1	0.333333333	2007.000000	-	2010.774320
107	K3PE3E300A	2010	1	0.333333333	2007.000000	-	2010.774320
108	K3PE3E300A	2010	1	0.333333333	2007.000000	-	2010.774320
109	MT46H256M32R4JV-6 WT	2011	1.441441441	1.201201201	2007.000000	-	-
110	MT46H256M32R4JV-5 WT	2011	1.2	1	2007.000000	-	-
111	MT42L128M32D1LF-25 WT	2011	1.110833333	0.333333333	2007.000000	-	2010.774320
112	MT42L32M16D1AB-25 WT	2011	1.110833333	0.333333333	2007.000000	-	2010.774320
113	MT42L128M64D2LL-25 WT	2011	1.110833333	0.333333333	2007.000000	-	2010.774320
114	MT42L128M32D1LH-18 WT	2011	1	0.250156348	2007.000000	-	2011.760513
115	MT42L128M64D2MP-18 WT	2011	1	0.250156348	2007.000000	-	2011.760513
116	MT42L256M32D2LG-18 WT	2011	1	0.250156348	2007.000000	-	2011.760513
117	MT48H16M32LFB5-75 IT	2011	3.609022556	3.007518797	2007.000000	-	-
118	K4X1G163PF	2011	1.2	1	2007.000000	-	-
119	K4X1G323PF	2011	1.2	1	2007.000000	-	-
120	K4X51163PK	2011	1.2	1	2007.000000	-	-
121	K4P8G304EC	2011	1.110833333	0.333333333	2007.000000	-	2010.774320
122	K3PE0E00M	2011	1.110833333	0.333333333	2007.000000	-	2010.774320
123	MT48H16M32LFB5-6 AAT	2012	2.874251497	2.395209581	2007.000000	-	-
124	K4P2G324ED	2012	1	0.250156348	2007.000000	-	2011.760513
125	K3PE4E700A	2012	1	0.250156348	2007.000000	-	2011.760513
126	K3PE4E400P	2012	1	0.250156348	2007.000000	-	2011.760513
127	K3PE7E700M	2012	1	0.250156348	2007.000000	-	2011.760513
128	K4PAG304EB	2012	1	0.250156348	2007.000000	-	2011.760513