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Technician Staffing for Intel – A Linear Programming Model

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Executive Summary/Abstract

This research is being submitted to show the use of Linear Programming to determine a staffing problem for Intel Corporation in one of the Ronler Acres factories in Hillsboro, Oregon. One of Intel's factories in Ronler Acres campus has increased factory capacity to make room to produce the next 14 nm technology process. The amount of manufacturing personnel needs to increase in order to make up for the increased amount of tools in the new factory space while still maintaining "lean manufacturing". In this paper we attempt to solve a problem by coming up with a minimum personnel number from the manufacturing side for one of Intel's factories in Hillsboro, Oregon since the number of tools for the next technology has increased, the amount of process operations have increased and the factory space has expanded.

The results of this research show how the use of a linear program is effective at providing a minimum staffing model in order to fulfill the job responsibilities of two types of groups, Manufacturing Technicians and Engineering Technicians.

Introduction

Background

Intel Corporation is the largest semiconductor manufacturer in the world, headquartered in Santa Clara, California. The company employs approximately 105, 000 people in its eleven fabrication facilities and six assembly and test facilities around the world, which have combined advanced chip design capability with a leading-edge manufacturing capability. Here in Oregon, Intel is the largest private employer in the state of Oregon with 17,000 employees in its R&D centers in Hillsboro, which makes up about 16% of Intel's global workforce. [1]

Intel is the inventor of the x86 series of microprocessors, the processors found in most personal computers. Intel Corporation was founded in July 18, 1968 by semiconductor pioneers Robert Noyce, Gordon Moore, and widely associated with the executive leadership and vision of Andrew Grove. Intel also makes motherboard chipsets, network interface controllers and integrated circuits, flash memory, graphic chips, embedded processors and other devices related to communications and computing.

One of Intel's major investments is in R&D. What makes Intel the biggest chip manufacturing company is keeping up with rapid changes in the microprocessor industry and constantly investing in R&D. Intel is number 4 in the list of top 10 spending R&D Companies at $8.4 billion in R&D spending in 2012 [2].

Intel has invested a big portion of its revenue in R&D. In the year 2012, Intel released its first 22nm tri-gate technology called "IVY Bridge". Intel is the first one to have come up with the 22nm technology after 10 years of research. Up until now, transistor layouts were "planar" or flat, in relation to the die. As Skaugen, Intel's head of PC client, says "the difference here is that 3D tri-gate transistors enable us to pack significantly higher transistor density on the die, helping increase the chips' performance and energy efficiency."[3] Each processor contains over 1.4 billion transistors. The process has become so difficult that to go even smaller to 14nm next year and reducing the power to half; it will be a great challenge.

Intel has its own collaborative partnerships with research centers, universities, and other companies. In fact, Intel is working on its next 450mm wafer manufacturing Intel labs in NY and partnerships with Google, Samsung and IBM. Intel's mission is to form a US-based research consortium that is looking into ways to move to bigger, next generation wafers.[4] Going from 300mm to 450mm wafer, means increasing tremendously equipment size and cost, but it will allow building more chips per wafer at a lower cost. "Intel hopes the agreement will shorten the timeline to create bigger and more cost-efficient 450-millimeter (mm) wafers and a new generation of advanced extreme ultraviolet lithography."[5] For this reason Intel is already building its manufacturing factories now, including D1X in Hillsboro where Mod-1 completion ended in 2012, and Mod-2 is already breaking ground this year, where 450mm wafer technology will start, as well as 2 other new fabs, Fab 42 in Arizona, and Fab 28 in Israel.

Figure 1Intel's Future Factories [7]

The way Intel is able to do this and continue to keep up with new innovation in such a rapid market is by having its factory ability and continuous upgrade. Intel is also preparing to upgrade fabrication plants in the United States and Ireland to make chips using the 14nm fab method. [6] Intel's R&D is quite deep and looks decades in advance. If it all goes to plan, Intel would start shipping 10nm processors in 2015. [7] In order to stay a few steps ahead of the competition, process technology is not the only key to the customer puzzle. Intel will also have to break into the mobile space with powerful, but energy-efficient chips.

Moore's Law

Intel co-founder Gordon E. Moore postulated in his famous 1965 paper that the number of components in integrated circuits had doubled every year from their invention in 1958 until 1965, and then predicted that the trend would continue for at least ten years. Later, David House, an Intel colleague, after factoring in the increase in performance of transistors, concluded that integrated circuits would double in performance every 18 months [8]. Soon after the realization of Moore's law, the suspicion on this law reaching an end persisted. Now, the concern is as serious as it can get. Not only has the feature size to be scaled down, the manufacturing cost also has to be contained. At the core of it are the lithography tools and processes to sustain Moore's law of scaling and Moore's law of economy. It includes the three viable candidates to push lithography beyond the 20nm logic node. In 1975, Moore refined his component count estimation to a doubling every two years, and thus a reduced exponential growth compared to his

initial estimation. Indeed, looking at the history of integrated circuits from 1975 to 2008, a doubling of transistor counts every two years was a good estimation [8]. This prediction known as Moore's Law has become a business-dictum for the whole semiconductor industry [8].

This source is from 1999 and back then it predicted that in 2010 we would be at one billion transistors per chip. Just last year, in 2012 with Intel's new 3rd Generation Intel Core, the 22nm 3-D technology named "IVY Bridge" has surpassed that prediction with 1.4 billion transistors in each processor [9]. For almost 50 years, the transistors used to fabricate chips have been flat, or planar. With the new 3-D Tri-gate structure, the transistors are formed on very tall and very skinny silicon "fins," with current flowing along the top and along the sides of these fins. The result is that these new transistors provide significantly improved energy efficiency, especially at low operating voltages, and increase the chips' performance. Intel is the first company to offer these new transistors and it took almost ten years of research.

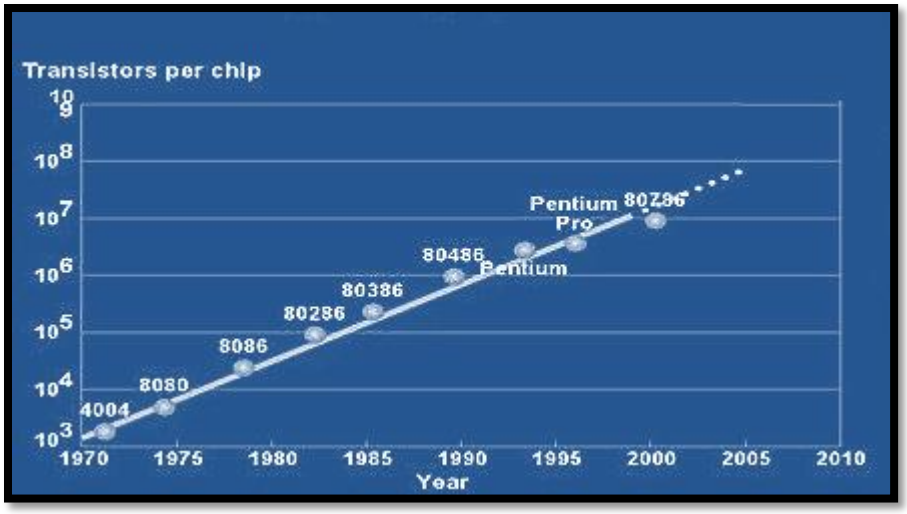

Figure 2 Illustrates the amount of transistors per chip through the years—publically available [8]

Problem Statement

Due to the high cost in manufacturing, smaller chip sizes that was undreamed of, and keeping up with Moore's Law, Intel is in critical position to accommodate all these challenges with the staffing it needs. Originally to keep up with these changes, we wanted to solve a staffing problem for Manufacturing Technicians due to increased number of tools and command stations for this next process technology. Due to IP restrictions, it was suggested that we try to solve the

personnel problem only on one part (one module) of the factory and that is Wet Etch module. They need to increase their amount of equipment by 41% of new tools. With that, there are 2 types of job roles, Manufacturing Technician (MT) whose job responsibility is to run operations and coordinate command stations, and Manufacturing Engineering Technician (MET) whose job role is to work on equipment maintenance and support Engineering experiments. Both roles need to support new training on the next process technology and train each other. Another change is that the amount of command stations needs to increase because the amounts of tool sets have increased. How many new command center stations will need to be figured out based on the amount of the new types of tool sets? These tool sets are divided between Front End (FE) and Back End (BE) Process and they need to be configured a certain way on these stations in order for MTs to do their job. Based on this, we can determine the minimum amount of new personnel we need to increase in order to support the next process technology development. Another factor that comes into effect is personnel cost since there are 4 different compressed work shifts operating 24/7. Night shift which includes 2 shifts has a greater cost in pay.

Wet Etch Process

People that work in the FAB are called Manufacturing Technicians. Technicians use computer workstations to perform and monitor manufacturing operations. These workstations are known as command centers. Many activities monitored by the technician are automated, including:

- Processing Lots
- Statistical Process Control
- Tool Performance Tracking
- Spec user "Read and Understand" status

The FAB which is contained in a cleanroom is divided into different areas known as "Functional Areas" and within each functional area are "Modules." Each functional area plays an important function in the process of making a microchip. Some functional areas to mention are:

- Diffusion
- Implant
- Thin Films
- Planar
- Litho
- Etch
- C4
- Sort

Within each functional area are modules. For example, Wet Etch and Dry Etch are 2 modules with the Etch functional area. Wafers pass through each Functional Area many times and in varying sequences to produce die. This is referred as the "Process Flow". [11]
The functional areas of Diffusion, Thin Films, Planar, Litho, Implant, and Etch complete the basic process of placing transistors into wafers. The wafers pass back and forth between these areas to manufacture die. In the Etch area, layers of material are "removed" to etch the circuit pattern onto the wafer.

Etch is one of the functional areas where the pattern created in Litho is transferred to the wafer by etching into the underlying layer of oxide, poly silicon, nitride or metal. These materials which are not covered by resist are removed in one of two ways:

- Dry or Plasma Etch – In a vacuum chamber, plasma or ionized gas is used to remove material from the wafer.
- Wet Etch – In an automated wet station, chemicals (acid or acid solutions) are used to remove material.

In the Wet Etch process, acid or other chemicals are used to etch material from the wafer.
Material is etched by immersing the wafer in a tank filled with acid or base chemical. The type of chemical depends on the material etched.
Wet Etch uses include:

- Etch Whole Layers – Whole layers of films that are no longer needed are etched from the wafer (e.g. silicon nitride, types of flims).
- Clean the Wafer – Cleans the wafer, removing particles, organic/metallic, contaminants, and residual resist. Cleans are done before some thin film layers are deposited and after some etch and implant steps are finished.

One major drawback of wet etches is that they etch equally in both the vertical and horizontal direction, producing an isotropic profile.

Literature Review

Introduction to Linear Programming

Linear programming provides the ability to have goals and to know a path of correct decisions to take when faced with practical complex situations. Linear programming has created tools to solve real industrial problems with complex mathematical models, techniques for solving the models and the various models for executing the steps for software algorithms.

Linear programming is used throughout operations research and scientific management but also used by numerical analysts, mathematicians, and economists. Linear programming is also known as linear optimization which is used for the problem of maximization and minimization of the linear function specified by linear and non-negativity constraints. Generally, linear programming is the optimization of an outcome based for some set of constraints using a linear mathematical model.

Linear Programming Use in Operation Research

Linear Programming is a crucial part in the optimization theory and operations research. A common problem which is faced by managers is how to allocate the resources within the range of available tools, activities and projects. Generally, Linear Programming (LP) is a method of allocating the resources most efficiently and optimal way. It is also one of the most widely used tools in operations research [12]. Linear Programming has been a successful tool for decision making, most of the industries, financial and service organizations. Therefore, it refers in planning processes which allocate resources such as men, material, machine and capital making it the best possible way where costs are minimized and profits are maximized. In Linear Programming, these resources are known as decision variables. The important criteria is selecting the best values for the decision variables i.e, to maximize profits or minimize costs is known as the objective function. The limitations on resource availability are known as set of constraints. These can be used for the input-output model, the determination of shadow prices and so forth. Linear Programming can be solved using the simplex method in which variables may take on integer values known as integer programming.

Scheduling Literature Review

The industry has shown us that when dealing with staffing schedules, nurse scheduling has been greatly studied. From literature review, until the 1960s, scheduling tools consisted only of graphical devices such as Gantt chart. It was J.P. Howell who outlined the steps necessary to develop a cyclical schedule. [13] Howell's method is a step-by-step procedure for accommodating the work patterns and individual preferences of nurses. In the early 1970s, scheduling systems began to be based on heuristic models [14] and [15]. Nowadays, various studies continue to be done on nurse scheduling, replacing the long manual hours of scheduling in various countries. One to mention uses a model that is approached through a 0-1 linear goal program. [16] It schedules nurses in a cyclical way, taking into account hard and soft constraints since the problem of satisfying every nurse's preference and still accommodating hospital's regulations, it is of great complexity.

As literature shows various researches on nurse staffing schedules, there is none published on technician staffing similar to the needs of our paper. Meanwhile, there have been plenty of publications that involve hierarchical decision making tools to aid the development of algorithms for real-time decision-making where disruptive events such as machine failures, material absences, expedited items, engineering changes, fluctuations of demand, and setups occur often. [17]

Current Model

The current setup that Intel chose is that there are a total of 13 Manufacturing Technicians (MTs) to run the 6 command centers (CC) per shift. Six MT's will be assigned to the backend (BE) tool sets and seven MT's assigned to the front end (FE) tool sets. In the event of staffing issues each of the CC's except tool set R, MTs should be able to cover all tools i.e.: All MTs in the FE process of the Wet Etch Module can cover between 3 command centers since they are all cross trained. Similar with the BE process. In addition to the MTs, there are Engineering Technicians (ET), they are trained on specific tool sets and are used for engineering support such has qualifications and machine maintenance.

Currently this module operates on 4 shifts for the hourly employees:

- Shift 1 day works Sunday through Tuesday from 7:30am – 8pm, and every other Wednesday.

- Shift 2 day works Thursday through Saturday 7:30am – 8pm and every other Wednesday.
- Shift 3 night works Sunday to Tuesday from 7:30pm – 8am and every other Saturday.
- Shift 4 night works Wednesday to Friday from 7:30pm – 8 am and every other Saturday.
- *Each shift overlaps half an hour for pass down meetings to each shift. Below is a table that illustrates a 2 week working period with rotations among the 4 shifts:

	WEEK 1							WEEK 2						
	SUN	MON	TUE	WED	THUR	FRI	SAT	SUN	MON	TUE	WED	THUR	FRI	SAT
SHIFT 1 DAY	7:30AM	7:30AM	7:30AM					7:30AM	7:30AM	7:30AM	7:30AM			
	8:00PM	8:00PM	8:00PM					8:00PM	8:00PM	8:00PM	8:00PM			
SHIFT 2 DAY					7:30AM	7:30AM	7:30AM				7:30AM	7:30AM	7:30AM	7:30AM
					8:00PM	8:00PM	8:00PM				8:00PM	8:00PM	8:00PM	8:00PM
SHIFT 3 NIGHT	7:30PM	7:30PM	7:30PM				7:30PM	7:30PM	7:30PM	7:30PM				
	8:00AM	8:00AM	8:00AM				8:00AM	8:00AM	8:00AM	8:00AM				
SHIFT 4 NIGHT				7:30PM	7:30PM	7:30PM					7:30PM	7:30PM	7:30PM	7:30PM
				8:00AM	8:00AM	8:00AM					8:00AM	8:00AM	8:00AM	8:00AM

Table 1Week Compressed Work Week Schedule

A challenge for payroll comes in for compressed work week hourly employees as there are certain guidelines by state. For the State of Oregon, the work week where employee has worked only 3 consecutive days of 12 hour shift equaling to 36 hours, 6 hours of that (meaning 2 hours each day) are considered Overtime pay plus an additional 5.9% on top of the base pay for those hours. A table is illustrated below.

12 hrs Shift	CWW Schedule	Straight Time Hours	Overtime Hours	Base Pay Rate	CWW Premium on Straight Time and Overtime Pay 5.9%
OR	3 Day CWW	30.0	6.0	$ 10.00	$ 17.70 / OT $3.54
	4 Day CWW	40.0	8.0	$ 10.00	$ 23.60 / OT $4.72

Table 2 CWW Pay

Another difference is that night shift, shift 3 and 4 get an additional 16% pay differential compared to day shifts 1 and 2.

Intel's hourly rates for MTs are as follows:

- Average Rate for Manufacturing Technicians per hour : $ 25.00
- Benefits (applies only to employees) : 16% of regular rate differential for night shift: 5.9% differential for CWW (compressed work week)
- Overtime (applies only to employees) : 1.5 of regular rate
- Regular Rate for Engineering Technicians on Average per hour: $31.00
- An eligible compressed workweek (CWW) is defined as any schedule that requires the employee to work 11.5 hours or more in a day. The CWW schedule premium applies to base straight-time hours and overtime hours and Intel pays this to non-exempt employees working an eligible schedule. CWW schedule premium is calculated as a state-based percentage (examples: CA 4.8%; OR 5.9%; others 6.5%) of base straight-time hours multiplied by your base hourly rate. Then, the state-based percentage of overtime hours is multiplied by your base hourly rate.
- Intel pays a compressed workweek (CWW) schedule premium to all nonexempt employees working a CWW schedule. The premium is intended to provide an incentive to nonexempt employees to work CWW schedules to support a business need. A CWW schedule premium is paid according to the schedule an employee works.

Constraints

There are certain restrictions for hourly employees in Oregon that they cannot work more than 13 hours in a given 24 hour period. Second restriction is for hourly Intel employees that cannot work more than 6 consecutive days.

Given:

- A technician cannot be assigned to more than one shift per day
- A technician working on evening shift cannot be assigned to the day shift the following day
- A technician assigned to a night shift must not be assigned to a shift of another type the next day.
- Limited number of successive work days 6

The current model of how each command center (out of 6 main ones) is configured below between the Front End and Back End process. Also due to IP, each tool set within the Wet Etch

module is being coded (CC1 contains toolset S and N, CC2 is E and G, CC3 is FP, CC4 is BP, CC5 is T, B, C and CC6 is R.)

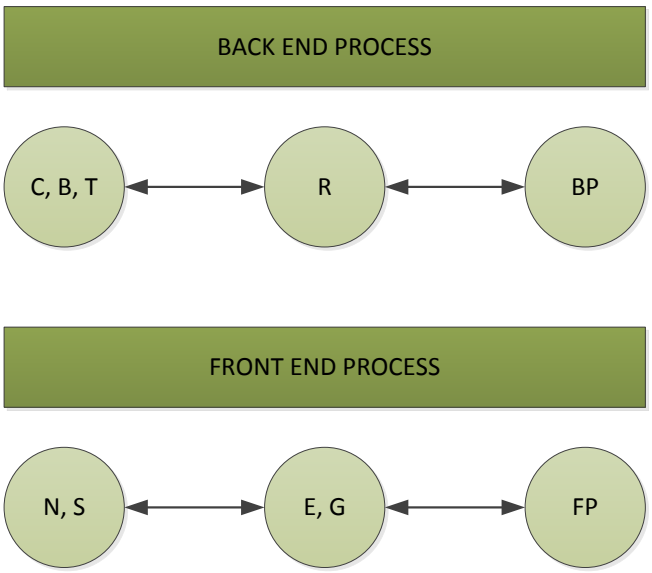

Figure 3 Current CC Configuration

Engineering Technician Staffing Training:

Current Intel's model is the 9 ETs trained for L1 Operations as explained below (due to IP restrictions, the types of toolsets are being coded):

For the Front End process there are:

- 1 ET for Toolset S and there are a total of 10 tools for both processes that this technician is responsible for.
- 1 ET for Toolset E and N, and there are 7 tools combined. Toolset N is also new for the new technology process.
- 1 ET for Toolset G and there are 5 tools combined.
- 2 ETs for Toolset FP/BP but they are in the same family of tools, only that one set supports Non Copper process, and the other set supports Copper.

For the Back End process there are:

- 2 ETs for toolset B/C/T and there are 21 tools combined.
- 2 ETs for toolset R and there are 14 combined.

Proposed Model

After looking into the constraints of Intel's current model, our team determined there is a more cost effective model which will still satisfy all the constraints of the scheduling process.

Objective

The main objective of our model is to discover a more cost effective model that minimizes the scheduling and staffing of MTs and ETs to command centers. We plan to achieve this by using Microsoft Solver to optimize the assignments of the 10 Toolsets to the 6 Command Centers based on the following:

- Toolsets are assigned to command centers to allowing a single ET to cover for the MT when necessary. ETs are Level 1 operation certified and part of their job expectations is to be able to run the command center and cover staffing when MTs are not available. ETs are limited in tool set knowledge as oppose to a MT.
- Minimizing the number of staffed MTs.

The goal is to minimize the number of MTs required per shift. Currently the proposed number of MTs per shift is 13; our target is less than this number. This is to allow a MT to operator each CC, as well as cover a MT when necessary for example breaks. We plan on achieving this goal by taking advantage of the 6 types of ETs available to operator the command centers. Each type of ET is certified and trained for specific tool sets. If the model can optimize the command centers to where an ET can operator the command center individually, instead of having another MT to cover, that would allow less MTs to be staffed per shift.

Decision Variables

The decision variables are the 10 Toolsets that can be arrange in any combination to the 6 command centers. The 10 Toolsets are the following:

- Toolset N
- Toolset S
- Toolset E
- Toolset G
- Toolset FP
- Toolset BP
- Toolset R
- Toolset C
- Toolset B
- Toolset T

The command centers will be labeled as the following:

- CC1
- CC2
- CC3
- CC4
- CC5
- CC6

Objective Function

The objective function is to minimize the sum of the tool sets assigned to the command centers.

$$Minimize \sum T_{ij}$$

Constraints

There are various constraints in our model given by our sources at Intel Corporation. The constraints are described below along with their mathematical notations.

1. An ET has a fixed set of skills. There are 6 different types of ET, each with specific skillset. They cannot learn new skills. The 6 types of Engineering Technicians are:

   E_1 is trained for operating Toolset S

   E_2 is trained for operating Toolset E and N

   E_3 is trained for operating Toolset G

   E_4 is trained for operating Toolset FP and BP

   E_5 is trained for operating Toolset B, C, and T

   E_6 is trained for operating Toolset R
2. There are 6 command centers that must be utilized. This is built into the decision variables.
3. There are 10 different Toolsets that must be utilized. This is built into the decision variables.
4. There is a minimum of 1 and a maximum of 3 Toolsets per command center.

$$1 \leq \sum_{i=1}^{6} \sum_{j=1}^{10} T_{ij} \leq 3$$

Tool set type *'i'* assigned to Command Center *'j'*

5. Each tool set should be assigned.

$$T_i \geq 1, \forall\, i$$

Tool set type *'i'* must be assigned to a Command Center

6. Decision variables are binary.

Results

Microsoft Solver was use to optimize the assignment of the Toolset to Command Centers. The solving method was Simplex LP. The Solver found a solution. All constraints and optimality conditions are satisfied.

The optimize assignment of the 10 Toolsets to the 6 Command Centers are as following:

- CC1 is assigned Toolset BP
- CC2 is assigned Toolset R
- CC3 is assigned Toolset C, B and T
- CC4 is assigned Toolset S
- CC5 is assigned Toolset G
- CC6 is assigned Toolset N and E

The new configuration for the 6 command centers is also described below in Figure 5.

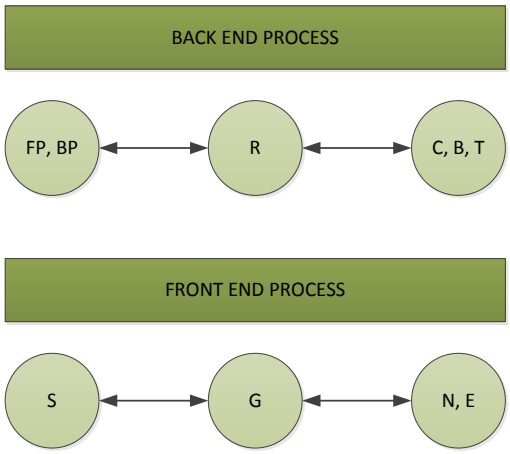

Figure 5. Our Propose CC Configuration

Discussion/Conclusion

Our first original idea was to see if we could minimize both MTs and ETs staffing in night shift since it has greater pay differential but we ran into a bigger problem; the way the command centers were setup, were not matching with ETs skillsets. One of the job responsibilities for the ETs, as mentioned earlier, is to be level 1 command center certified and to be able to help when MT staffing is insufficient. The optimization model did just that for us. It configured command centers based on ETs skillsets. The outcome of this model also allows for an MT to operate each of the command stations. We originally started this model knowing Intel's current model that

they planned on hiring 3 new MTs and 1 new ET for the new process technology in the upcoming year due to increased amount of operations, tools, and command centers. They were planning on going from 10 MTs and 8 ETs to 13 MTs and 9 ETs. We found that the new command center configurations needed to be redone based on skillset and that satisfies our model.

Current Intel regulations are that each command station needs an MT to operate it at all times. Oregon law is that in a working 12.5 hour shift, an employee needs total breaks equaling to 2.5 hours. That means that someone needs to break each MT from each command station. This is where ETs come in based on their certified training to perform this job duty. Second restriction is that in a team of 8 MTs, 2 are allowed to be on vacation at the same time. Thus our minimum amount of 6 MTs need to be increased to 8. This still means a reduction of 5 less MTs compared to Intel's original plan. The required time for breaks will be utilized by the ETs performing that job function. The number of ETs stays unchanged. In this way, this model suggests saving Intel 5 MT headcount in just 1 shift in only one module, the Wet Etch module. From Intel finance group, it costs Intel on average $100,000 a year per technician employee (including wages, benefits, desk space etc). This model suggests saving Intel $2 million a year from just one module from only one factory across four operating shifts.

Recommendations

This study validated that Linear Programming can be a valuable tool for managers when assigning staffing to specific job tasks with minimizing the amount of recourses, in this case, people. For future studies, it will be beneficial to recommend this model to Intel, test it out, and possibly implement it. It could be suggested that the model gets tested in the original module that we started in Wet Etch, and then to get tested in other modules. Due to timing, if this model does not benefit Intel for the upcoming year, it could be useful to be looked at in future decisions when looking at technician staffing. In this project, we did have a few limitations; one worth mentioning is that only Solver was used as the optimization tool. In the future, other programs could be useful.

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Appendix

Excel Implementation

The decision variables are setup in a matrix with toolsets in the X-Axis and command centers in the Y-Axis. The Solver will assign the 10 toolsets to the 6 command centers subject to the constraints.

Decision Variables										
	Tool N	Tool S	Tool E	Tool G	Tool FP	Tool BP	Tool R	Tool C	Tool B	Tool T
CC1	0	1	0	0	0	0	0	0	0	0
CC2	0	0	0	1	0	0	0	0	0	0
CC3	0	0	0	0	0	0	1	0	0	0
CC4	1	0	1	0	0	0	0	0	0	0
CC5	0	0	0	0	0	0	0	1	1	1
CC6	0	0	0	0	1	1	0	0	0	0

The Objective Function is set to make sure all the toolsets are utilized.

Objective Function		
	Sum of All Toolset	10

Constraint 1 describes each of the ET type and their respective skillset. ET typically have one or more skillsets. For ETs with more than one skill set, the value was divided by the number. This allowed the total to sum to one, meaning one ET.

Constraint 1										
	Tool N	Tool S	Tool E	Tool G	Tool FP	Tool BP	Tool R	Tool C	Tool B	Tool T
ET1		1								
ET2	0.5		0.5							
ET3				1						
ET4					0.5	0.5				
ET5								0.33	0.33	0.34
ET6							1			

Constraint 3 sums the usage of each toolset and checks to make sure they are used just once. The LHS is the sum of the row for each toolset.

Constraint 3											LHS		RHS
Toolset N	1										1	=	1
Toolset S		1									1	=	1
Toolset E			1								1	=	1
Toolset G				1							1	=	1
Toolset FP					1						1	=	1
Toolset BP						1					1	=	1
Toolset R							1				1	=	1
Toolset C								1			1	=	1
Toolset B									1		1	=	1
Toolset T										1	1	=	1

Constraint 4 sums the number of toolsets assigned to each command center and check to make sure it is less than or equal to 3.

Constraint 4									LHS		RHS
CC1 Toolset Maximum									1	<=	3
CC2 Toolset Maximum									1	<=	3
CC3 Toolset Maximum									1	<=	3
CC4 Toolset Maximum									2	<=	3
CC5 Toolset Maximum									3	<=	3
CC6 Toolset Maximum									2	<=	3

Constraint 5 has two parts, labeled 5A and 5B. 5B is used to supplement 5A. 5B contains a list of all the possible combinations of toolset to command centers. 5B sums each ET per command center and check to make sure they are greater or equal to one.

Constraint 5A									LHS		RHS
CC1 Toolset									1	>=	1
CC2 Toolset									1	>=	1
CC3 Toolset									1	>=	1
CC4 Toolset									1	>=	1
CC5 Toolset									1	>=	1
CC6 Toolset									1	>=	1

Constraint 5B											LHS
CC1-ET1	0	1	0	0	0	0	0	0	0	0	1
CC1-ET2	0	0	0	0	0	0	0	0	0	0	0
CC1-ET3	0	0	0	0	0	0	0	0	0	0	0
CC1-ET4	0	0	0	0	0	0	0	0	0	0	0
CC1-ET5	0	0	0	0	0	0	0	0	0	0	0
CC1-ET6	0	0	0	0	0	0	0	0	0	0	0
CC2-ET1	0	0	0	0	0	0	0	0	0	0	0
CC2-ET2	0	0	0	0	0	0	0	0	0	0	0
CC2-ET3	0	0	0	1	0	0	0	0	0	0	1
CC2-ET4	0	0	0	0	0	0	0	0	0	0	0
CC2-ET5	0	0	0	0	0	0	0	0	0	0	0
CC2-ET6	0	0	0	0	0	0	0	0	0	0	0
CC3-ET1	0	0	0	0	0	0	0	0	0	0	0
CC3-ET2	0	0	0	0	0	0	0	0	0	0	0
CC3-ET3	0	0	0	0	0	0	0	0	0	0	0
CC3-ET4	0	0	0	0	0	0	0	0	0	0	0
CC3-ET5	0	0	0	0	0	0	0	0	0	0	0
CC3-ET6	0	0	0	0	0	0	1	0	0	0	1

CC4-ET1	0	0	0	0	0	0	0	0	0	0	0
CC4-ET2	0.5	0	0.5	0	0	0	0	0	0	0	1
CC4-ET3	0	0	0	0	0	0	0	0	0	0	0
CC4-ET4	0	0	0	0	0	0	0	0	0	0	0
CC4-ET5	0	0	0	0	0	0	0	0	0	0	0
CC4-ET6	0	0	0	0	0	0	0	0	0	0	0
CC5-ET1	0	0	0	0	0	0	0	0	0	0	0
CC5-ET2	0	0	0	0	0	0	0	0	0	0	0
CC5-ET3	0	0	0	0	0	0	0	0	0	0	0
CC5-ET4	0	0	0	0	0	0	0	0	0	0	0
CC5-ET5	0	0	0	0	0	0	0	0.33	0.33	0.34	1
CC5-ET6	0	0	0	0	0	0	0	0	0	0	0
CC6-ET1	0	0	0	0	0	0	0	0	0	0	0
CC6-ET2	0	0	0	0	0	0	0	0	0	0	0
CC6-ET3	0	0	0	0	0	0	0	0	0	0	0
CC6-ET4	0	0	0	0	0.5	0.5	0	0	0	0	1
CC6-ET5	0	0	0	0	0	0	0	0	0	0	0
CC6-ET6	0	0	0	0	0	0	0	0	0	0	0

Solver configuration

Set Objective: $E$13

By Changing Variable Cells: $C$5:$L$10

Subject to the Constrainsts:

$C$5:$L$10 = binary, decision variables set to binary

$M$63:$M$68 >= $O$63:$O$68, constraint 5

$M$71:$M$80 = 1, constraint 3

$M$83:$M$88 <= $O$83:$O$88, constraint 4