Title: SEC-Reactor Deposition Model Simulation

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EMGT 510-TERM PROJECT

SEC-REACTOR DEPOSITION MODEL SIMULATION

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ABSTRACT

Sec, is a manufacturer of silicon and epitaxial wafers. In this Project we want to develop a simulation model to study the processing flow of different sizes of epitaxial wafers through the deposition process.
In this model we study two different processing alternatives, for different types of wafers, in order to maximize overall profit during one week of production.

INTRODUCTION

Sec, is a manufacturer of raw material used in the production of integrated circuits. Sec, produces Silicon wafers ranging in diameter from 4" to 6" with a total of three different types of products.

In Sec's epitaxial manufacturing process , raw material necessary for the process arrives two times per day in volumeof units big enough to cover 24 hours of production and is stored in the wharehouse. This company stores enough inventory for two days of production. Sixty percent of all the wafers are precleaned in three different units and are later sent to the lot formation station with all the remaining wafers.

In the lot formation station each different type of wafer is organized in lots of different sizes which are later sent to the different reactors. The simulation model will focus on these two processes. The whole process flow diagram is shown included with the model description.

PROBLEM DEFINITION

Sec manufactures bare silicon wafers and epitaxial coated wafers used in the manufacture of integrated circuits. This project is focused on the simulation on the epitaxial deposition process. The deposition process is done in three different types of reactors classified as type A, B, and C. Type A and type B reactors can not process 6" wafers and type C reactors can not process 4" wafers.

Product Flow

Input	Reactor Type	Output
4" Wafers	A	4" Wafers 5" Wafers
5" Wafers	B	4"Wafers 5"Wafers
6" Wafers	C	5"Wafers 6"Wafers

The net profit per lot size for each type of wafer processed varies depending on the type of reactor.The information for the different lot sizes and lot net profits is given below:

Lot Size Matrix (units)

Type of:	Reactor		
Product	A	B	C
4" Wafer	21	23	-
5" Wafer	11	11	17
6"Wafer	-	-	14

Net Profit Per Processed Lot ($Dollars)

Type of:		Reactor	
Product	A	B	C
4" Wafer	3.99	4.37	-
5" Wafer	2.97	2.97	4.59
6" Wafer			5.88

The objective of this simulation model is to increase the net profit generated in the deposition process by simulating different alternatives of processing different types of wafer lots.

MODEL FORMULATION

The main elements of the model needed to simulate the deposition manufacturing process are shown below. This are the main elements necessary to build the model in Promodel.

Locations:

The locations in our model are the lot formation station, the three queues necessary to organize the three different types of wafer lots, and the three different type of reactors.

Entities:

The entities of the model are the different types of wafer lots coming to each reactor.

Arrivals:

The arrival rates (interrarrival time between one oncoming lot and the next) are different for each reactor type depending on the type of lot being processed. (See Table). The arrival rates are assummed independent.(IID)

Arrival Process

Log Normally Distributed

Type:		Reactor	
Product	A	B	C
4"	Mean=0.17757	Mean=0.08643	-
	Std. Dev.=0.45398	Std.Dev.=0.2086	-
5"	Mean=0.09285	Mean=0.08980	Mean=0.09797
	Std.Dev.=0.16598	Std.Dev.=0.1647	Std.dev=0.2746
6"	-	-	Mean=0.07044
	-	-	Std.Dev=0.17155

Processing:

The operation at each different type of reactor varies depending on the type of wafer being processed (See Table).

Processing Distributions

Type:		Reactor	
Product	A	B	C
4"	Gamma Distribution	Pearson Type 6(a,b,c)	-
	Shape parameter=1.175	a=1,b=2,c=1	-
	Scale parameter=2.035		
5"	The same Gamma	The same Pearson	Exponential(E)
	Distribution	Type 6	Mean(E)=2.28829
6"	-	-	Log-Normal
	-	-	Mean=3.2548
			Variance=98.8684

SIMULATION ALTERNATIVES PROPOSED

The following two alternatives are proposed to process the different types of wafers:

1. Process Alternative:

All the wafers are processed on a firstcome - first serve basis. We define three queues for all the oncoming types of wafer lots.

2. Process Alternative:

All the wafers are processed in three different queues and are processed according to the following priorities:

a) 4" Wafer lots are processed first in reactors type A and B.

b) 6" Wafer lots are processed first in reactors type C.

C)5" Wafer lots are processed after 4" and 6" wafer queues are empty.

DATA ANALYSIS

Data Collection:

The processing rates were taken for each of the eleven reactors actually operating in the shop floor

and all the data times collected classified by type of reactor and wafer lot type. The processing times were taken as the time in hours between units leaving the deposition process.

Similarly the times between arrivals at each of the reactors was taken for each type of wafer lot. All of the time collected was later classified and sorted by type of reactor and type of wafer lot.

Data Analysis

The times between arrivals and departures from each type of reactor is continuous . All of the data was analyzed using unifit and the following steps.

Step1. The statistical data parameters- Data sample statistics was calculated. The sample statistics includes mean, variance, coefficient of variation , lexis ratio and skewness factor.

Step2. The different available continuous distributions available in the unifit program were fitted with the measured data and ranked according to maximum likelihood.

Step3. A histogram comparison of the data collected and the best ranked model was analyzed.

Step4. The best ranked model was tested using the Chi-square Goodness of fit test was performed and the table results of the test were analyze for the different levels of significance.

Step5. The quantile table summaries and box-plots were performed to analyze the data and visualize existing outliers.

The analysis of the data suggests that both the time between arrivals and processing(departures)

are not fitted by any of the continuous distributions offered in unifit and must be fitted using empirical distributions.

Further analysis shows that the data variance values are large compared to the mean values of the data sample summary statistics showing a great dispersion of the random variables about the mean.

An analysis of the box-plot shows that the data collected presents an over aggregation of the data over a small portion of the overall range of values of the random variables. These outliers must be studied to understand their causes and possible solution to problems in the flow of the wafers through the deposition process.

For the purpose of our model , however , we assumed that both the data of arrival times and the processing times are continuously distributed because the models objective is to show different ways of organizing the processing priorities depending on the type of wafer lot , to increase the net profit of the process. The model does not actually want to represent the actual system behavior, and rather depicts only three of the
eleven reactors.

VERIFICATION OF THE SIMULATION PROJECT

A detailed verification of the simulation model is not possible at this point because the model itself has not been programmed and is only conceptually stated. The programming flow logic can not be verified yet.

VALIDATION PROCESS

The concept behind this model is to simulate a given set of three different type of reactors and processing the wafer lot types according to the different priority rules, in order to increase the net profit generated in the deposition process.

A validation process can be carried on based on the results given by the proposed simulation model. The l results can be used later on to schedule production in three selected reactors type A, B and C according to the processing priorities set in the conceptual model. The results of the experiment would be compared with the expected outcome of the conceptual model in order to validate its application.

PROJECT HISTORY AND CONCLUSIONS

The project was developed under a very limited time frame. The general steps of the modeling process ; problem definition, data collection, and model conceptualization were analyzed and developed but the expected simulation model is not yet developed.

The most important mistake was not identifying a project on time. Another mistake was not interacting with the Promodel program earlier in the beginning of the first two weeks of the course.

BIBLIOGRAPHY

1. Averill M. Law, W. David Kelton, "Simulation Modeling & Analysis",Second Edition, Mac Graw Hill, US., 1982

2. ProModel for Windows, Version 1.05, Users Manual, Promodel Corporation, 1993

3. Averill M. Law, Stephen G. Vincent,"unifit II-User's Guide",Averill M.Law &Associates, 1993